CPU 72x

Table of Contents

1. Processor Modules CPU 72x 2
1.1 Overview 2
1.2 Extension Bus and Dimensions 4
1.3 Extensibility 7
1.4 Terminal Assignment 8
1.5 Configuration CPU 72x 14
1.6 System Behavior 19
1.7 Technical Data 24
1.8 Accessories: Flash Cassette FMC 701-T 29

List of Figures

Fig.01: MOBI bus: extension bus plug (view from front) 4
Fig.02: Dimensions CPU 72x 4
Fig.03: Processor module CPU 723-T 5
Fig.04: Processor modules CPU 725-LT/LTH, CPU 727-T/TH 6
Fig.05: Extensibility CPU 72x 7
Fig.06: Terminal assignment CPU 723-T 8
Fig.07: Terminal assignment CPU 725-LT/LTH and CPU 727-T/TH 8
Fig.08: Wiring of power supply (UC) 9
Fig.09: CAN bus wiring 10
Fig.10: RS-232C wiring 11
Fig.11: Connection of the CPU 723-T digital input 12
Fig.12: Connection of the CPU 723-T digital output 12
Fig.13: Connection digital inputs CPU 725-LT/LTH and CPU 727-T/TH 13
Fig.14: Connection digital outputs CPU 725-LT/LTH and CPU 727-T/TH 13
Fig.15: Memory map CPU 72x 17
Fig.16: LEDs CPU 723-T, CPU 725-LT/LTH and CPU 727-T/TH 19
Fig.17: Battery backup time of the CPU 72x-Tx/CTx 23
Fig.18: Connection diagram digital inputs 26
Fig.19: Connection diagram interrupt inputs 27
Fig.20: Connection diagram digital outputs 28
Fig.21: Dimensions flash cassette FMC 701-T 29
Fig.22: Mounting the flash cassette 29

1. Processor Modules CPU 72x

1.1 Overview

The CPU 72x decentralized processor modules cover the following functions:

- CPU in closed housing (IP40) for mounting on DIN rail
- Communication via CAN bus and RS-232 interface
- Can be extended with digital and analog extension modules
- I/O interfaces with analog or digital inputs/outputs
- FMC 701-T memory cassette with CPU 72x as an option
- Programming in IEC 61131-3

1.1.1 List of Modules

The following decentralized CPUs 72x are available to the user:

CPU	723-T	725-LT	725-LTH	727-T	727-TH
Flash-EPROM 512 kB		×	×		
Flash-EPROM 1 MB	×			×	×
Serial EEPROM 2kB	×	×	×	×	×
Slot for optional Flash cassette	×			×	×
RAM 256 kB		×	×		
RAM 1 MB	×			×	×
RAM buffer	×			×	×
with RTC	×			×	×
without RTC		×	×		
1 CAN interface		×	×	×	×
2 CAN interfaces	×				
analog peripheral					
digital peripheral	×	×	×	×	×

RTC: Real Time Clock with buffered battery.

1.1.2 Inputs and Outputs

The CPUs 72x have the following inputs and outputs:

CPU 723-T	Number	Galvanically isolated from the logic system
Digital inputs 24 Vdc	4	Yes
Digital inputs 24 Vdc	2 with f_C = 25kHz [1)]	Yes
Digital outputs 24 Vdc / 0.5 A	4	Yes

[1)] f_C: critical frequency

CPU 725-LT, CPU 727-T	Number	Galvanically isolated from the logic system
Digital inputs 24 Vdc	8	Yes
Digital outputs 24 Vdc / 0.5 A	8	Yes

CPU 725-LTH, CPU 727-TH	Number	Galvanically isolated from the logic system
Digital inputs 36 Vdc	8	Yes
Digital outputs 36 Vdc / 0.5 A	8	Yes

1.2 Extension Bus and Dimensions

1.2.1 Extension Bus

On the right-hand side of the front of the units, there are connection plugs for the MOBI bus, by means of which the extension modules are connected.

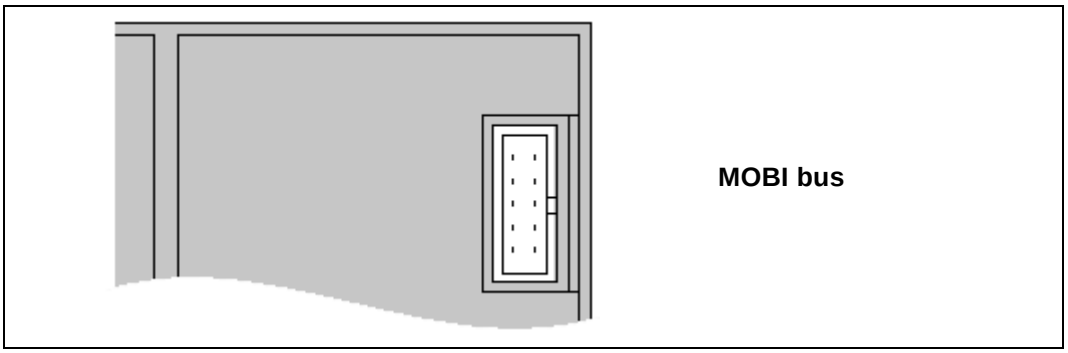


Fig.01: MOBI bus: extension bus plug (view from front)

1.2.2 Dimensions

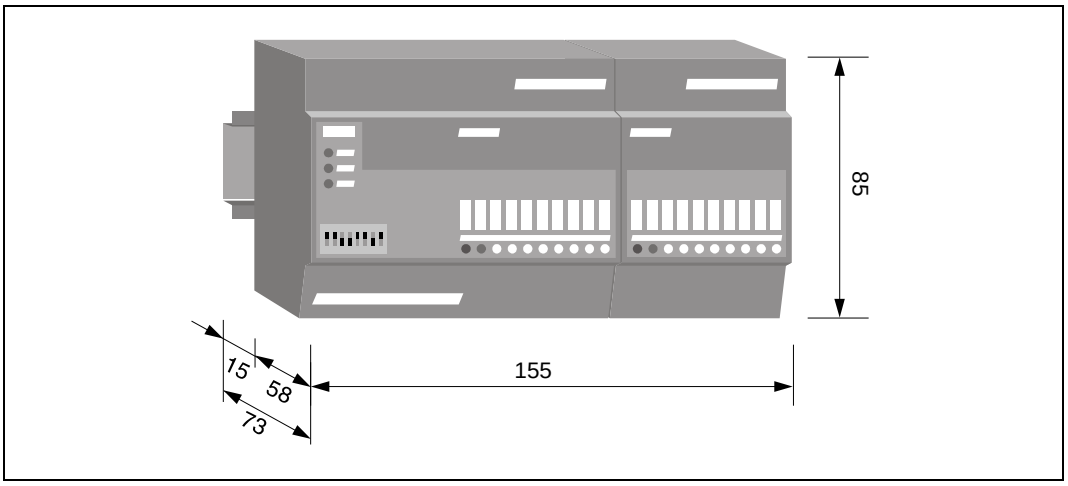


Fig.02: Dimensions CPU 72x

1.2.3 Processor Module CPU 723-T

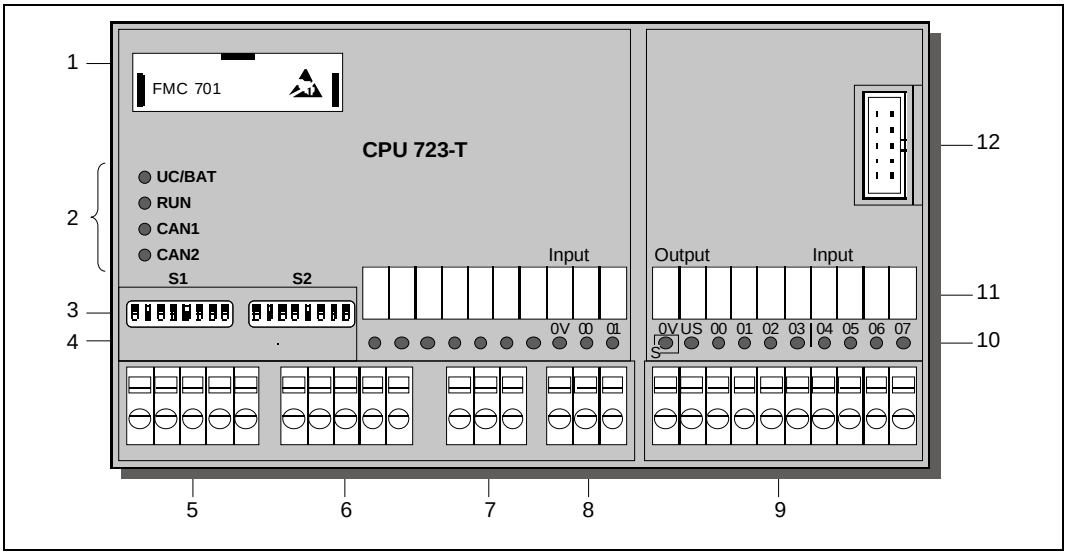


Fig.03: Processor module CPU 723-T

Legend:

1:	Slot for Flash cassette
2:	LEDs: UC/BAT: Power supply and lithium accumulator/battery status RUN: CPU operation mode CAN1: CAN communication on CAN bus 1 CAN2: CAN communication on CAN bus 2 S: Short circuit on the digital output
3:	DIP switch S1 for CAN bus: Adjustment of the CAN bit rate and the node address
4:	DIP switch S2 for CPU configuration: Adjustment of the start-up behavior and the RS-232C
5:	Connector for CAN bus 1 and power supply (UC)
6:	Connector for CAN bus 2
7:	Connector for RS-232C
8:	Terminal strips for digital inputs
9:	Terminal strips for digital inputs and outputs
10:	LEDs
11:	Labeling strips
12:	Link connector for subsequent extension modules

1.2.4 Processor Modules CPU 725-LT/LTH, CPU 727-T/TH

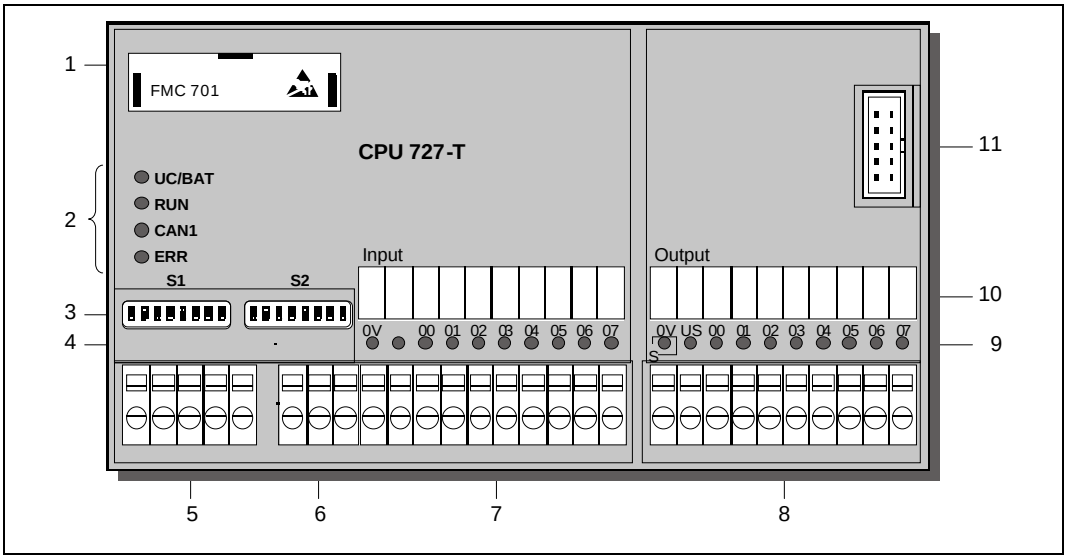


Fig.04: Processor modules CPU 725-LT/LTH, CPU 727-T/TH

Legend:

1:	Slot for Flash cassette
2:	LEDs: UC / BAT: Power supply and lithium accumulator/battery status RUN: CPU operation mode CAN: CAN communication on CAN bus ERR: Error S: Short circuit on the digital output
3:	DIP switch S1 for CAN bus: Adjustment of the CAN bit rate and the node address
4:	DIP switch S2 for CPU configuration: Adjustment of the start-up behavior and the RS-232C
5:	Connector for CAN bus 1 and power supply (UC)
6:	Connector for RS-232C
7:	Terminal strips for digital inputs
8:	Terminal strips for digital inputs and outputs
9:	LEDs
10:	Labeling strips
11:	Link connector for subsequent extension modules

1.3 Extensibility

All CPU 72xs can be expanded with the following modules.

- DIT 70x Extension modules with digital inputs
- DOT 70x Extension modules with digital outputs
- DDT 70x Extension modules with digital inputs and outputs

- AIT 70x Extension modules with analog inputs
- AOT 70x Extension modules with analog outputs
- PWT 70x Extension modules with PWM outputs

The upper limit for extension modules is 6.
(Consider maximum power consumption of the extension modules. See chapter "Extension Modules MAS 72x", 1.2 Power Consumption on the MOBI Bus.)

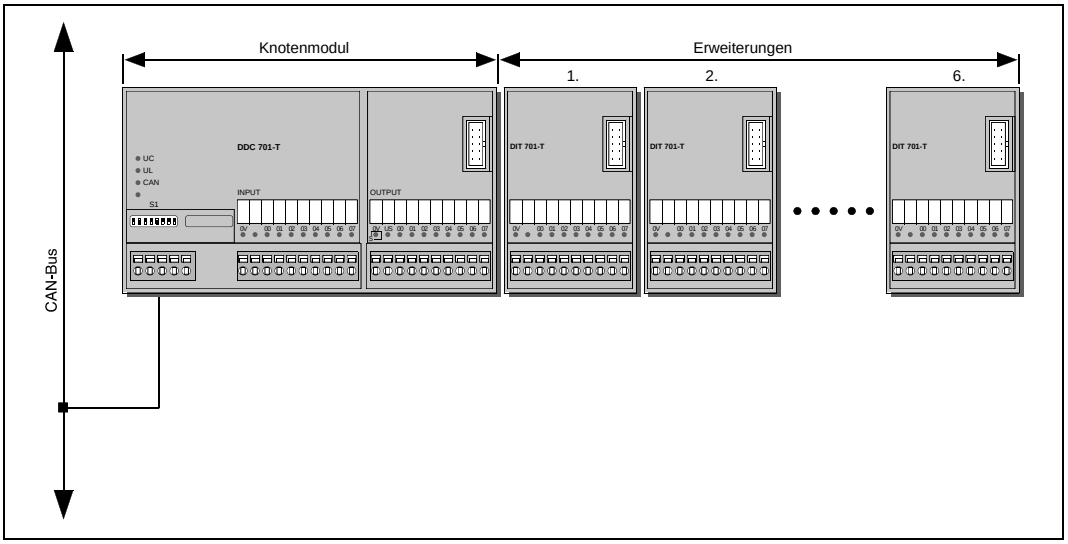


Fig.05: Extensibility CPU 72x

IMPORTANT

Never connect and disconnect extension modules when the unit is live, since this may result in irreparable damage to the module.

1.4 Terminal Assignment

1.4.1 Overview

1.4.1.1 CPU 723-T

The CPU 723-T is wired via two 5-pole, two 3-pole and one 10-pole connectors.

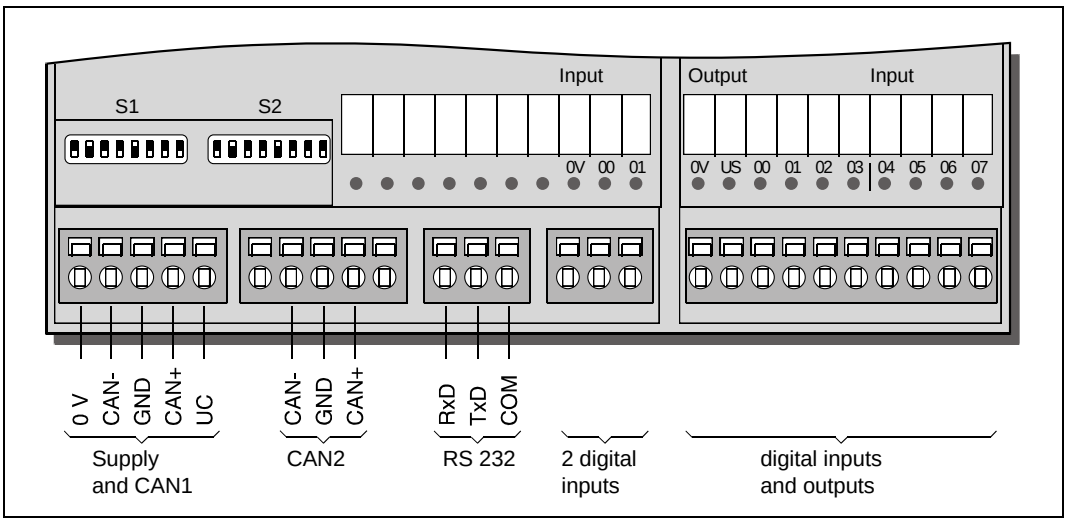


Fig.06: Terminal assignment CPU 723-T

1.4.1.2 CPU 725-LT/LTH, CPU 727-T/TH

CPUs CPU 725-LT/LTH and CPU 727-T/TH are wired by means of one 5-pole, one 3-pole and two 10-pole connectors:

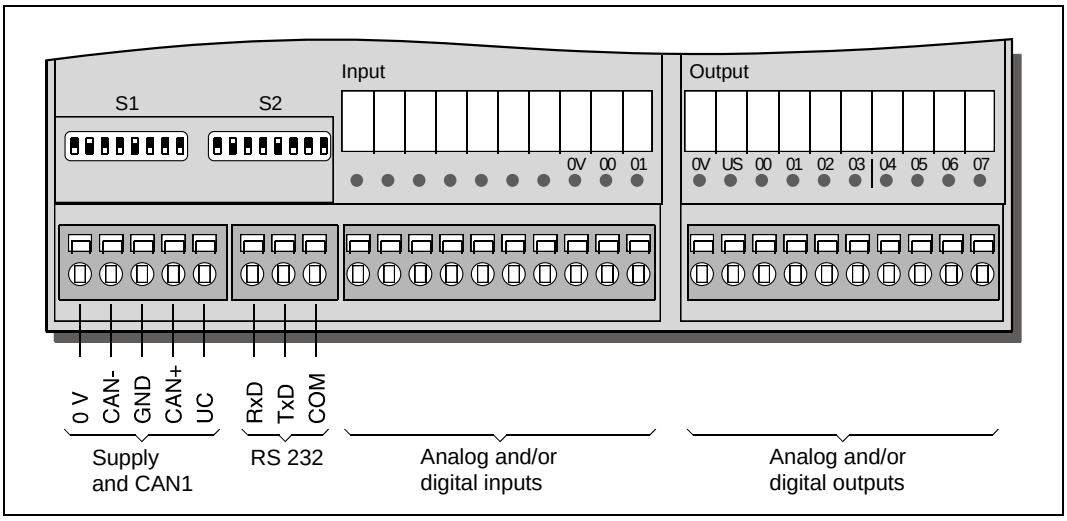


Fig.07: Terminal assignment CPU 725-LT/LTH and CPU 727-T/TH

1.4.2 Power Supply

The 24 Vdc power supply of the CPU 72x is realized via the 5 pole connecting terminal (UC and 0V). Via the extension bus the internal 5 Vdc logic supply (UL) is connected to the extension modules.

Power Supply CPU 72x	**-T/LT**	**-TH/LTH**
Power supply UC		
Nominal value	24 Vdc	36 Vdc
Limit value	16.8…30.0 Vdc	25.2…45.0 Vdc
Powerfail threshold typ.	16 Vdc	17 Vdc
Power consumption CPU without extension modules	2.6 W	2.6 W
Max. power consumption CPU with extension modules	11 W	11 W
Max. power supply for extension modules	5 W	5 W
Galvanic separation		
UC ↔ logic	Yes [1)]	Yes [1)]
UC ↔ CAN supply	Yes [1)]	Yes [1)]
Logic ↔ CAN supply at CPU 725/727	Yes	Yes
Logic ↔ CAN1 supply at CPU 723-T	No	—
Logic ↔ CAN2 supply at CPU 723-T	Yes	—
against ground	Yes [1)]	Yes [1)]
Test voltage	560 Vac, 800 Vdc	
Powerfail error	Yes, if UC < Powerfail threshold, the LED ‘UC’ goes out	

[1)] simple insulation

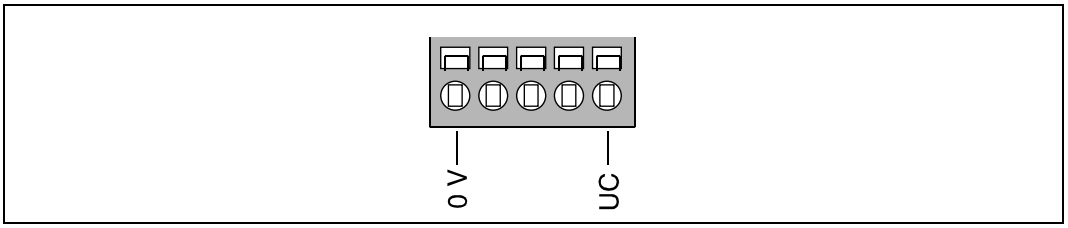


Fig.08: Wiring of power supply (UC)

1.4.3 Interfaces

The decentralized processor modules CPU 72x are equipped with one (CPU 725-LT/LTH and CPU 727-T/TH) or two (CPU 723-T) CAN bus interface and one RS-232 interface.

1.4.3.1 CAN Bus

The connection of the CAN bus is realized via a 5 pole terminal (CAN-, GND and CAN+).

CAN Bus	CPU 723-T	CPU 727-T/TH	CPU 725-LT/LTH
Galvanic separation			
CAN1 ↔ logic	No	Yes [1)]	Yes [1)]
CAN1 ↔ RS-232C	Yes [1)]	Yes [1)]	Yes [1)]
CAN1 ↔ UC	Yes [1)]	Yes [1)]	Yes [1)]
CAN2 ↔ logic	Yes [1)]	—	—
CAN2 ↔ RS-232C	Yes [1)]	—	—
CAN2 ↔ UC	Yes [1)]	—	—
CAN ↔ ground	Yes [1)]	Yes [1)]	Yes [1)]
Test voltage	560 Vac, 800 Vdc		
Bit rates	setting via DIP switch S1 and/or software		
Max. bit rate			
CAN1	1 Mbit/s	500 kbit/s	500 kbit/s
CAN2	500 kbit/s	—	—
Driver	Level according ISO 11898 standard		

[1)] simple insulation

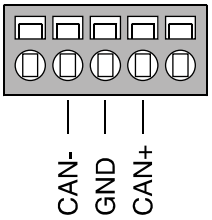


Fig.09: CAN bus wiring

Note

At the beginning and the end of the CAN bus network the terminal resistances RT = 120 Ω are to put in (see chapter "Installation, Startup, and Operation", 5.2.3 CAN Bus Termination).

1.4.3.2 RS-232C

The serial interface RS-232C can be used as data or programming interface.

The connection of the RS-232C interface ensues via the 3 pole connecting terminal (RXD, TXD and COM).

The maximum bit rate is 38.4 kbit/s.

RS-232C	CPU 723-T, CPU 725-LT/LTH and CPU 727-T/TH
Galvanic separation	
RS-232C ↔ logic	Yes [1)]
RS-232C ↔ CAN	Yes [1)]
RS-232C ↔ UC	Yes [1)]
RS-232C ↔ ground	Yes [1)]
Test voltage	560 Vac, 800 Vdc
Bit rates	setting via DIP switch S1 and/or software
Driver	Level according ISO 11898 standard

[1)] simple insulation

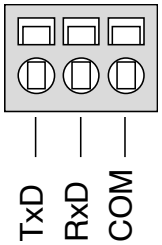


Fig.10: RS-232C wiring

1.4.3.2.1 Installation Remarks

To fulfill the EMC standards (89/336/EEC and EN 50081-2/EN 50082-1) the following point is to consider at wiring:

RS-232C cable screening to connect on a large area by means of the strain reducing clip of the CTA 703-T.

IMPORTANT

Do not connect screen on the peripheral side (e.g. PC) with the ground.

1.4.4 Inputs and Outputs

1.4.4.1 Connection of the CPU 723-T Digital Input

The CPU 723-T has six 24 Vdc digital inputs. The 00 and 01 inputs are interrupt inputs.

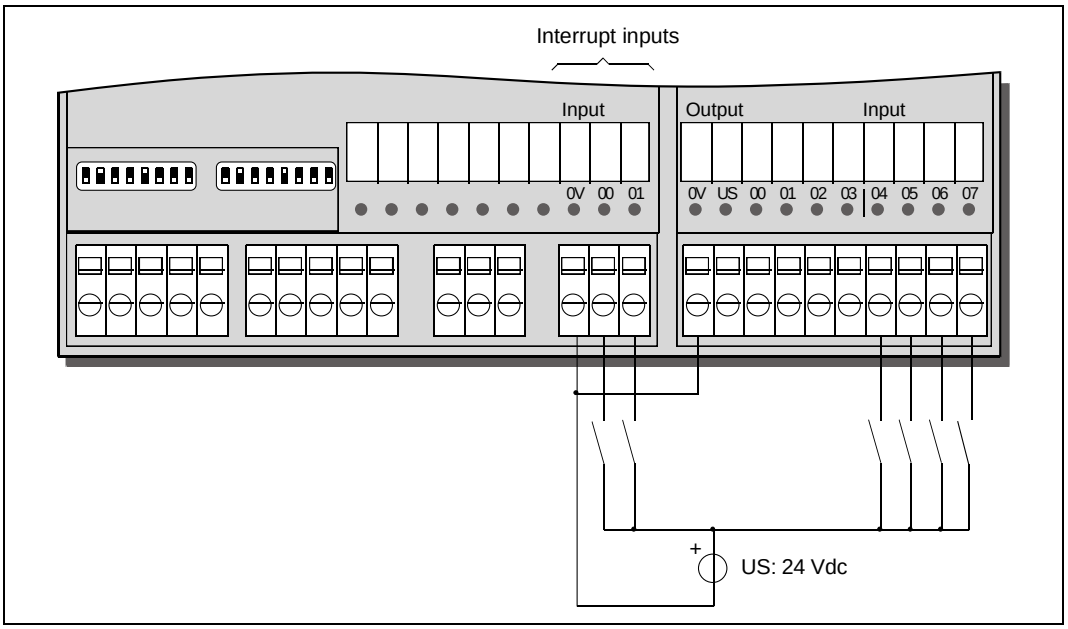


Fig.11: Connection of the CPU 723-T digital input

1.4.4.2 Connection of the CPU 723-T Digital Output

The CPU 723-T has four 24 Vdc / 0.5 A digital outputs.

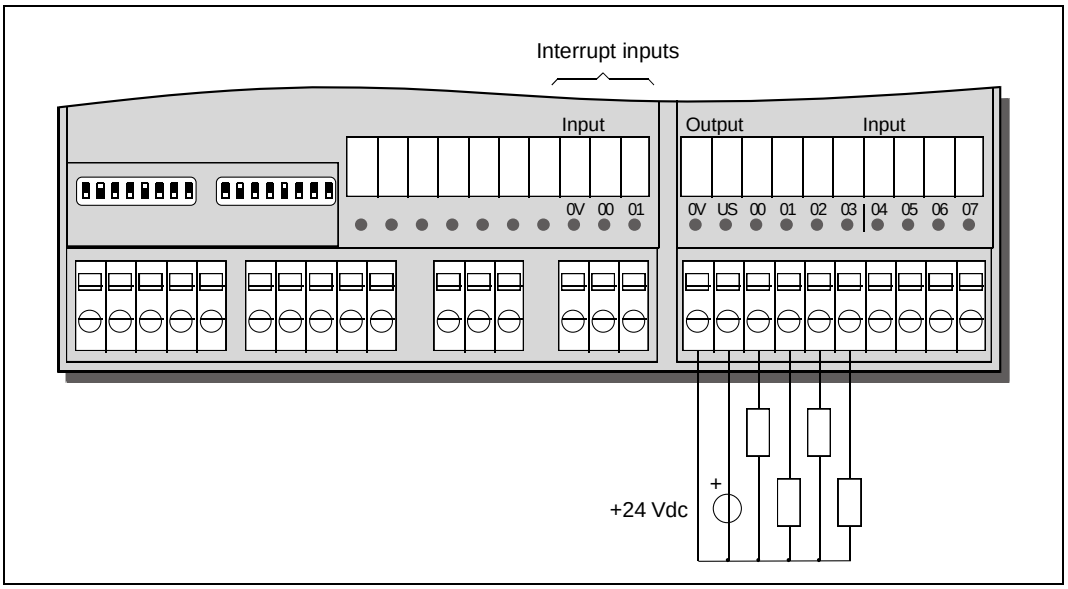


Fig.12: Connection of the CPU 723-T digital output

1.4.4.3 Connection of the CPU 725-LT/LTH and CPU 727-T/TH Digital Inputs

CPUs CPU 725-LT/LTH and CPU 727-T/TH have 8 digital inputs 24/36 Vdc.
These are galvanically isolated from the logic system and have a common 0 V connection.

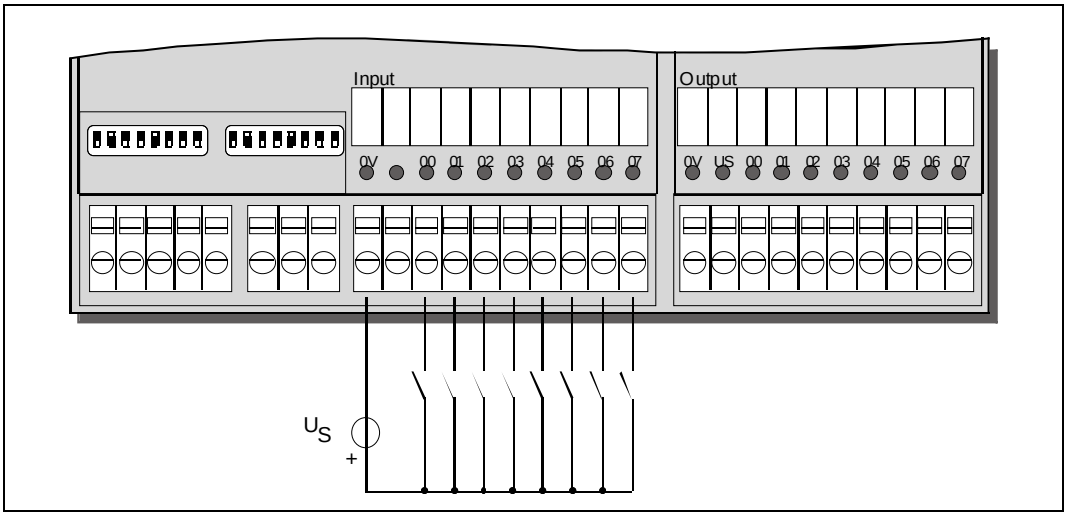


Fig.13: Connection digital inputs CPU 725-LT/LTH and CPU 727-T/TH

1.4.4.4 Connection of the CPU 725-LT/LTH and CPU 727-T/TH Digital Outputs

CPUs CPU 725-LT/LTH and CPU 727-T/TH have 8 digital outputs 24/36 Vdc / 0.5 A.
These are galvanically isolated from the logic system and have a common 0 V connection.

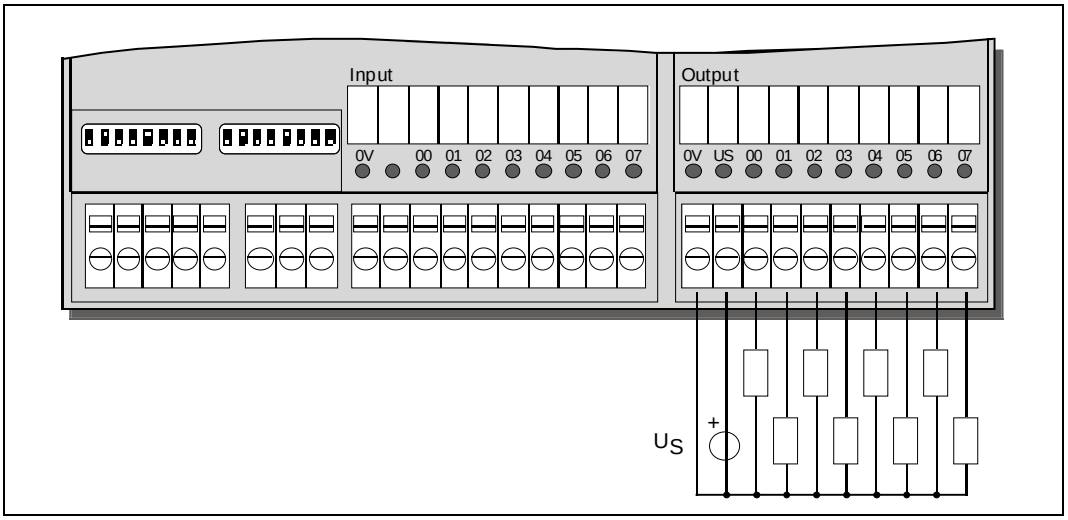


Fig.14: Connection digital outputs CPU 725-LT/LTH and CPU 727-T/TH

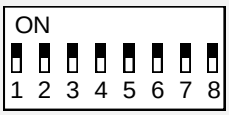
1.5 Configuration CPU 72x

On the CPU 72x are two DIP switches (S1 and S2) allowing the adjustment of the following points:

- Node address of the module
- CAN bus bit rate of the module (CAN 1 on CPU 723-T)
- Operation modes of the CPU
- Type of the RS-232 interface
- Bit rate of the RS-232 interface

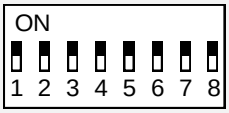
Note

The position of the DIP switches is only read at the start-up phase.

DIP Switch S1	Switch	Function
	1 to 5 and 8	CAN address
	6 and 7	CAN bus bit rate
	8	Switch bit 0…31 / bit 32…63

Note

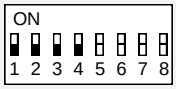
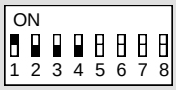
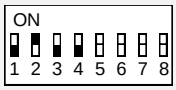
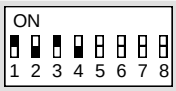
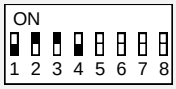
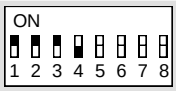
Settings see chapter "Installation, Startup, and Operation", 6.1 CAN Bus Configuration.

DIP Switch S2	Switch	Function
	1 to 4	Operation modes
	5	Type RS-232 interface
	6 and 7	RS-232 bit rate
	8	Special function with CPU 723-T: 0 = DIP switch S1 valid for CAN1 1 = DIP switch S1 valid for CAN2 The other CAN interface is set using the SW functions of the library SYSTEM_MLib can_hw_node_adr_n and can_hw_bitrate_n in the application program. The default settings are: Bit rate: 100 kbit/s Address: 0

1.5.1 Operation Modes

The operation modes of the decentralized processor modules are set by means of DIP switch S2 (DIP 1 to 4).

1.5.1.1 Start-Up Behavior

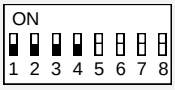
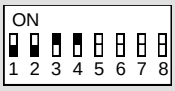
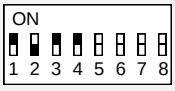
SW	CPU 72x (DIP Switch S2)	Fct. [1]	Auto-start	Program Start-Up from
1		C	No	RAM
2		C	Yes	RAM
3		C	Yes	Backup flash EPROM intern
4		C	Yes	Backup flash EPROM - external (cassette). The runtime system (RTS) is also started from the cassette if it has been copied by the user. Otherwise, the RTS is used by the internal flash.
5		W	No	RAM
6		W	Yes	RAM
7				
	CPU 723-T CPU 727-T/TH	W	Yes	Backup flash EPROM intern
	CPU 725-LT/LTH	C	Yes	Backup flash EPROM intern
8				
	CPU 723-T CPU 727-T/TH	W	Yes	Backup flash EPROM - external (cassette). Runtime system (RTS) as under SW 4
	CPU 725-LT/LTH	C	Yes	Backup flash EPROM - external (cassette). Runtime system (RTS) as under SW 4

[1] Fct; W: Warm start , C: Cold start

IMPORTANT

On DIP switch S2 the CPU 725-LT/LTH may only take the positions SW 1 and SW 3. Reason: The CPU 725-LT/LTH has no battery !

1.5.1.2 Service Functions

SW	CPU 72x (DIP Switch S2)	Function	
9		PROG:	Switch position for programming the CPU with software CAP1131.
10			Switch position for loading the run time system and application software from Flash memory cassette to the Flash EPROM.
11		DLD:	Switch position for loading the run time system into the Flash EPROM.

Note

Detailed information to the start-up behavior of the CPU 72x with and without Flash cassette can be taken in the "System Manual MAS Software", chapter "MAS Programming", 3.4 Operating statuses and startup behavior.

1.5.1.3 Memory Map CPU 72x

From the following memory map, it can be seen that two different memory sizes are distinguished with the CPU 72x:

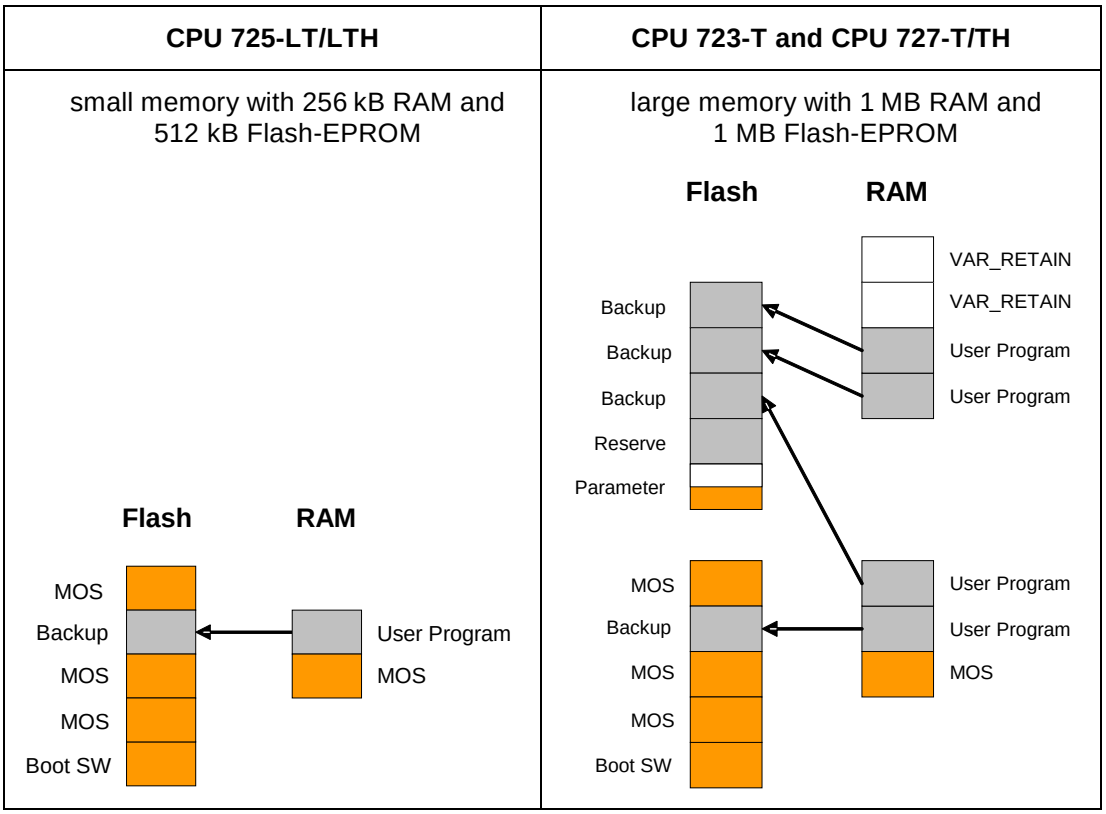


Fig.15: Memory map CPU 72x

Legend:

Boot SW	Boot software
MOS	MAS operating system
Backup	User program and data in flash EPROM
User Program	User program
VAR_RETAIN	Warm start variables
Parameter	Domain in flash EPROM for user parameters

IMPORTANT

With the small memory CPUs, when the 'Backup/Restore' function is executed in the CAP1131 programming tool, the whole RAM content is copied into the flash EPROM, i.e. the user program and the data. When the CPU is started up in operation mode RUNB, all variables (including warm start variables) are overwritten with the content of the variables in the flash EPROM!

1.5.1.4 Programming Instructions

The user program is loaded into RAM via the programming interface (see "System Manual MAS Software", chapter "MAS SW: CAP1131", 5. Program Compilation, Download, Online Change)

The RAM of the CPU 72x is buffered so that, in the event of a power failure, the user program and data are not lost.

Copy the user program after downloading into the CPU from the RAM in the flash EPROM (see "System Manual MAS Software", chapter "MAS SW: CAP1131", 6.9 Backup/Restore) so that RUNB mode (automatic startup of the program from flash EPROM) can be executed.

Copy the user-program after the download into the CPU:

- From RAM to the Flash EPROM [1)] for execute the operation modes SW 3 and SW 7 RUNB.
- From RAM to the external Flash EPROM 2 (cassette) for execute the operation modes SW 4 and SW 8.

[1)] See "System Manual MAS Software", chapter "MAS SW: CAP1131", 6.9 Backup/Restore

1.5.2 Interfaces

1.5.2.1 CAN Bus Connection

Note

See chapter "Installation, Startup, and Operation", 5.2.3 CAN Bus Termination.

1.5.2.2 RS-232C

The RS-232 interface can be used either as data or as programming interface.

The setting ensues by means of switch 5 of the DIP switch S2.

DIP Switch S2 5	Function
off	Data interface
ON	Programming interface (Load of the run time system, program download, monitoring)

1.5.2.2.1 Data Interface

As data interface the RS-232C allows the connection of any type of ASCII terminal for system diagnosis or data exchange with other units.

The bit rate is set via the application.

1.5.2.2.2 Programming Interface

If the RS-232C is used as programming interface, a PC with the program development system CAP1131 can be connected to this port.

The bit rate of the programming interface is set via the switches 6 and 7 of the DIP switch S2.

DIP Switch S2		Bit Rate
6	7	
off	off	9600 Bit/s
ON	off	19200 Bit/s
off	ON	38400 Bit/s

1.6 System Behavior

1.6.1 LED Functions

To display the operating status, the 72x CPUs have 4 LEDs on the front.

There are differences between the different types of CPU:

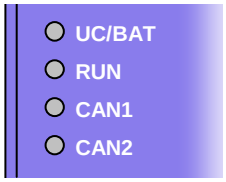
CPU 723-T	CPU 725-LT/LTH and CPU 727-T/TH
	

Fig.16: LEDs CPU 723-T, CPU 725-LT/LTH and CPU 727-T/TH

Legend:

LED		Color *)	Function
UC/BAT		gn, or + rd	UC power supply and battery monitor
RUN		gn, or + rd	CPU status and error display
CAN		gn + rd	CPU status and error display for µC defect
CAN1		gn + rd	Status of CAN bus 1
CAN2		gn + rd	Status of CAN bus 1
ERR		rd	Status of CAN bus 2

*) gn: green; or: orange; rd: red

LED UC/BAT

LED UC/BAT shows the status of the UC power supply and the charge status of the Li battery in the CPU 72x units.

LED status		Meaning
●	off	UC power supply < Powerfail threshold
●	green on	UC power supply good
●	orange on	UC power supply good and Low-Battery display
●	red on	UC power supply < Powerfail threshold and Low-Battery display

LED RUN

LED RUN displays the module status and the error status.

LED status		Meaning
●	off	User program stopped and no error
◐	green flashing	User program in Hold Mode
●	green on	User program running in RUN Mode
●	red on	Especially with CPU 723-T: the application has stopped and the Watch-Dog-Reset has come on or the µC is not running. Other 72x CPUs: the µC is not running.
◐	orange / red flashing	Application in Hold Mode and Watch-Dog-Reset is on.
●	orange on	Application in RUN Mode and Watch-Dog-Reset is on.
◐	red flashing	Fatal error.

LED CAN / CAN1

LED CAN / CAN1 displays the status of CAN communication on the first CAN bus.

LED status		Meaning
●	off	CAN / CAN 1 not active
◐	green flashing	More than 96 error reports have occurred in communication on the CAN bus, i.e. the warning limit has been reached.
●	green on	CAN / CAN 1 no error, normal operating status
●	red on	The CAN bus CAN / CAN 1 is in 'BUS OFF' state. No further CAN communication is possible. The CAN controller has switched off.

LED CAN2

LED CAN2 displays the status of CAN communication in the CPU 723-T on the second CAN bus.

LED status		Meaning
●	off	CAN 2 not active
●	green on	CAN 2 no error, normal operating status
◐	green flashing	Strongly disturbed data-transfer. The warning limit has been reached. CAN communication conditionally possible.
●	red on	The CAN bus CAN 2 is in 'BUS OFF' state. CAN communication is no longer possible. The CAN controller has switched off.

LED ERR

LED ERR displays the error status on the CPU 725-LT/LTH and on the CPU 727-T/TH.

LED status		Meaning
●	off	No error
●	red on	The Watch-Dog-Reset is occurred
◐	red flashing	Fatal error

The decentralized processor modules are trouble resistant according the IEC 61131 standards.

If other types of problems occur, the comportment of the CPU 72x is as follows:

1.6.2 Power Supply Breakdown (UC)

A powerfail is triggered if the supply voltage UC falls below the powerfail threshold U_{PF}.

Powerfail Threshold in the Versions…	CPU 72x-T/LT	CPU 72x-TH/LTH
Powerfail threshold (U_{PF}) typ.	16 Vdc	17 Vdc

The CPUs accept a power interruption of 10 ms (according IEC 61131-2 PS2) without any consequences.

If the supply voltage UC drops below 17 Vdc and the internal logic supply UL is still higher as 4.65 Vdc, then all outputs are switched off and the CPU waits, until the internal logic supply UL drops below 4.65 Vdc. The application is not executed anymore and the ‘ERR’-LED blinks. The application will only continue to work after a reset (UL < 4.65 Vdc).

When the internal logic supply UL will underpass UL 4.65 Vdc, a reset is released.

1.6.3 Overvoltage (UC and US)

The CPUs are protected against overvoltage peaks according the IEC 61131 standards. In cases that the supply voltage is continuously higher than indicated in the technical data, a destruction of the unit cannot be excluded.

1.6.4 Undervoltage (US)

If the power supply of the digital outputs underpasses 17 V, a power fail message is sent to the controller and the LED ‘US’ extinguishes. The outputs are switched off.

1.6.5 Cross-Polarity

The power supply UC is protected against cross-polarity, which is not the case for the power supply US.

1.6.6 Short Circuit

A short circuit at a digital output produces a switch off of all digital outputs of the module concerned and the red LED "S" lights on.

If an analog output is overcharged, the technical data cannot anymore be guaranteed. The outputs are however not damaged if the current does not exceed 30 mA (not short circuit proofed), no feedback message is generated.

1.6.7 RAM and RTC Buffering

WARNING

Non-rechargeable lithium battery

Injury from explosion

→ Under no circumstances recharge the lithium battery

The lithium battery RBA 721 has a capacity of 3.0 V, 190 mAh. Assuming a typical current consumption of 10 µA (at 25°C), this corresponds to a backup duration of 750 days. This value applies if the CPU is never connected to the supply voltage.

If the CPU is operated from the power supply for 12 h per day, for example, this results in a proportional increase in the backup time. In this case, the backup time is doubled to 4 years.

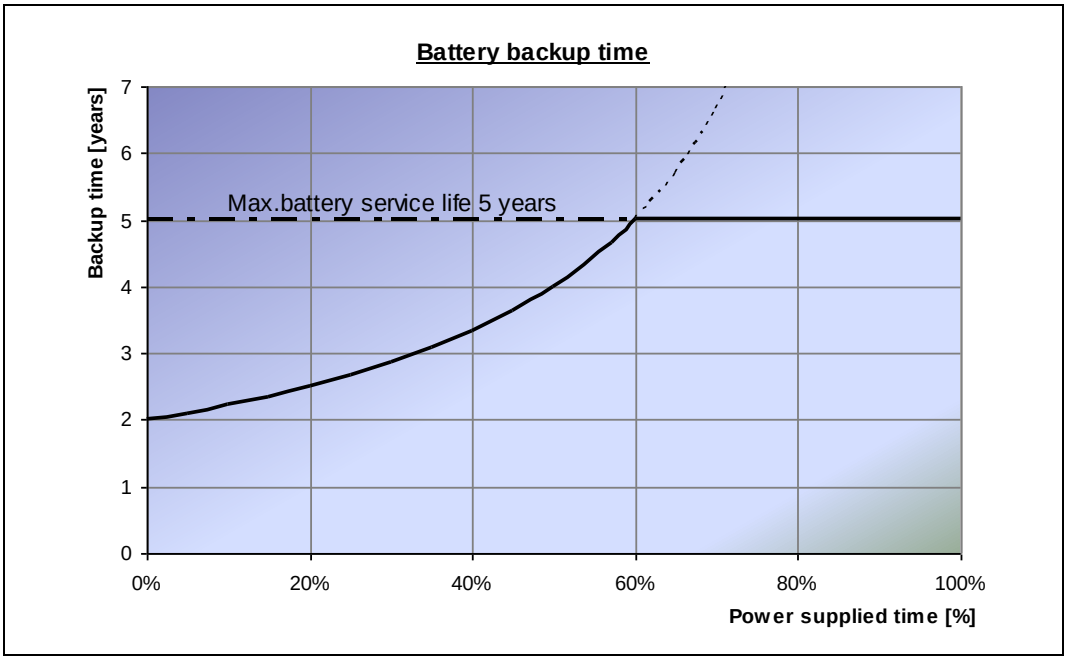


Fig.17: Battery backup time of the CPU 72x-Tx/CTx

IMPORTANT

- The service life of the battery is restricted to 5 years even given optimum backup.
- The battery must be renewed after 5 years even in devices that are in store.
- Typical current consumption at 25°C is 10 µA
  However, current consumption may vary between 5 µA and 40 µA depending on the temperature.

1.6.8 Startup Behavior

After switch on of the power supply the monitoring circuit activates the reset up to the voltage is stabilized (max. 50 ms after surpassing the level of 4.65 Vdc). As soon as this process is executed, the run time system starts in the Flash-EPROM.

1.7 Technical Data

1.7.1 General Data

Technical Data	CPU 723-T	CPU 725-LT	CPU 727-T
Overall failure rate [1)]	λ = 2018 FIT	λ = 3552 FIT	λ = 3552 FIT
Processor	80C167	80C167	80C167
Backup FEPROM	1 MB	512 kB	1 MB
of which available for user-program and data	896 kB	128 kB	896 kB
RAM memory	1 MB	256 kB	1 MB
serial EEPROM	2 kB	2 kB	2 kB
RAM buffered with lithium battery	Yes	No	Yes
Power supply			
Nominal value		24 Vdc	
Limits		16.8…30.0 Vdc	
Powerfail threshold		16 Vdc	
Power consumption typ.		2.6 W	
Communications interface for programming and data input / output		RS-232	
CAN interface	2	1	1
Digital inputs 24 Vdc	6	8	8
Digital outputs 24 Vdc / 0.5 A	4	8	8
Expandable with			
digital I/Os	Yes	Yes	Yes
analog I/Os	Yes	Yes	Yes
Slot for 1 MB flash cassette	Yes	No	Yes
RTC buffered	Yes	No	Yes
Ambient temperatures			
Operation		-25…+70°C	
Storage		-40…+85°C	
Index of protection		IP40	
Dimensions (W×H×D)		155 × 85 × 58 mm	
Weight		360 g	
Article no.	44120223	44120265	44120227

[1)] λ: Overall failure rate | $MTBF = \frac{10^9}{\lambda[FIT]}$; $\lambda[FIT] = \frac{10^9}{MTBF}$

Technical Data	CPU 725-LTH	CPU 727-TH
Overall failure rate [1)]	λ = 3552 FIT	λ = 3552 FIT
Processor	80C167	80C167
Backup FEPROM	512 kB	1 MB
of which available for user-program and data	128 kB	896 kB
RAM memory	256 kB	1 MB
serial EEPROM	2 kB	2 kB
RAM buffered with lithium battery	No	Yes
Power supply		
Nominal value	36 Vdc	
Limits	25.2…45.0 Vdc	
Powerfail threshold	17 Vdc	
Power consumption typ.	2.6 W	
Communications interface for programming and data input / output	RS-232	
CAN interface	1	
Digital inputs 36 Vdc	8	
Digital outputs 36 Vdc / 0.5 A	8	
Expandable with		
digital I/Os	Yes	Yes
analog I/Os	Yes	Yes
Slot for 1 MB flash cassette	No	Yes
RTC buffered	No	Yes
Ambient temperatures		
Operation	-25…+70°C	
Storage	-40…+85°C	
Index of protection	IP40	
Dimensions (W×H×D)	155 × 85 × 58 mm	
Weight	360 g	
Article no.	44120365	44120326

[1)] λ: Overall failure rate | $MTBF = \frac{10^9}{\lambda[FIT]}$; $\lambda[FIT] = \frac{10^9}{MTBF}$

Device-specific accessories

Article	Art.no.	Description
RBA 721	44170224	Replacement battery for CPU 72x-T (except CPU 727-DT)
TBA 710	44170016	Terminal block set for CPU 725/727 with spring terminals
TBA 720	44170033	Terminal block set for CPU 723-T with spring terminals
TBA 730	44570106	Connection terminal for CPU 72x and DDC 72x
FMC 701-T	44170232	Flash cassette with 1MB Flash EPROM

EMC Protection Circuitry between Power Supply and Earth

Detailed information regarding the EMC protection circuitry between power supply and earth connection is contained in the "System Manual MAS 72x", chapter "Installation, Startup, and Operation", 2.4 EMC Protection Circuitry between Power Supply and Earth Connection.

1.7.2 Technical Data - Inputs and Outputs

1.7.2.1 Digital Inputs

The normal digital inputs of the CPU 72x have the following input switching:

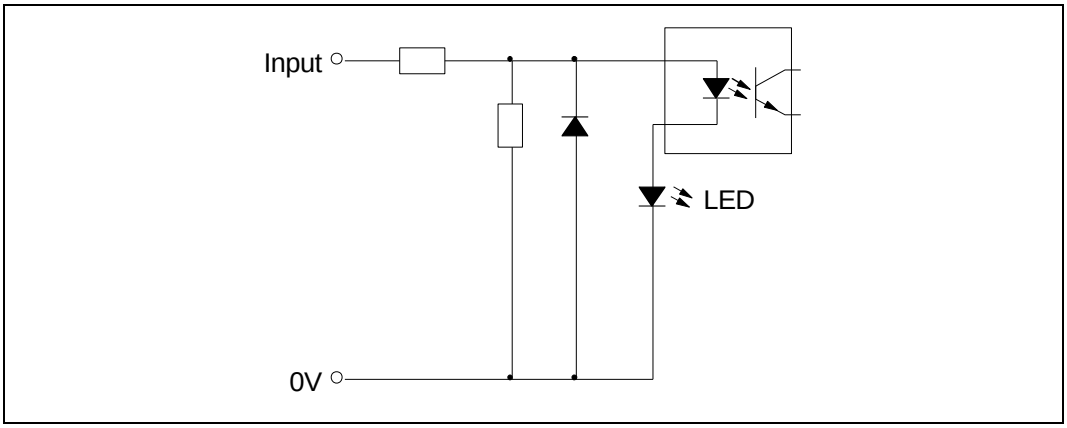


Fig.18: Connection diagram digital inputs

Legend:

Digital Inputs CPU 72x	**-T/LT**	**-TH/LTH**
Input type as per IEC 61131-2	Type 1	
Display	LED green, lights up with signal = 1	
Input voltage	0…24 Vdc	0…36 Vdc
Limits	-30.0…+30.0 Vdc	-45.0…+45.0 Vdc
for signal = 0	< 5 Vdc	< 7.5 Vdc
for signal = 1	> 14 Vdc	> 19 Vdc
Input resistance typ.	3.9 kΩ	6.8 kΩ
Input current with signal = 1 typ.	6 mA [1)]	5.3 mA [1)]
Input delay typ.	0.6 ms (input filter)	
Adjustable via software	5.6 ms	
Potential insulation		
Input ↔ logic	Yes, simple insulation	
Input ↔ input	No	
Effect with cross-polarity of inputs	No destruction, no high currents	

[1)] at UC = Nominal value

IMPORTANT

Paralleling of inputs **not** allowed!

1.7.2.2 Interrupt Inputs

The interrupt input of the CPU 723-T has the following input switching:

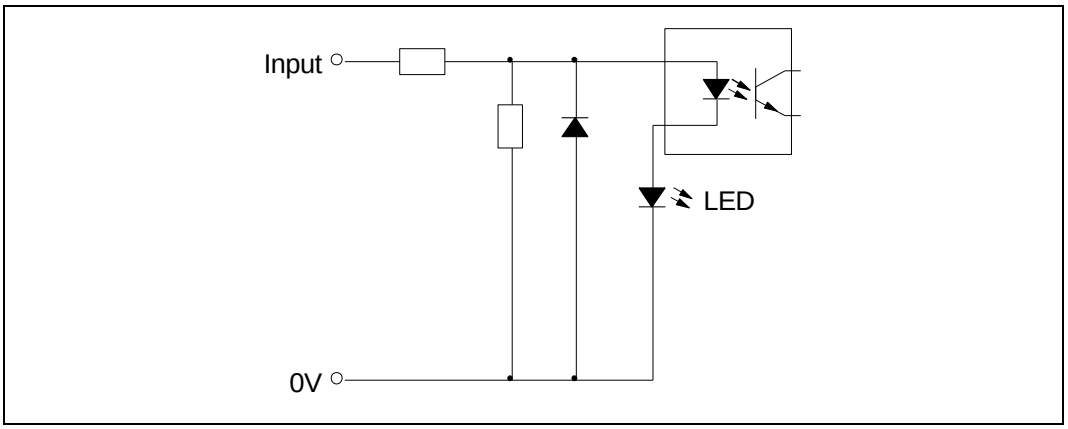


Fig.19: Connection diagram interrupt inputs

Legend:

Digital Interrupt Inputs CPU 723-T	
Input type as per IEC 61131-2	Type 1
Display	LED green, lights up with signal = 1
Input voltage	0…24 Vdc
Limits	-30.0…+30.0 Vdc
for signal = 0	< 5 Vdc
for signal = 1	> 14 Vdc
Input current with signal = 1 typ.	11 mA [1)]
Input resistance typ.	2 kΩ
Input delay typ.	0.6 µs
Input frequency max.	25 kHz
Switching edge distance	min. 10 µs
Galvanic separation	
Input ↔ logic	Yes, simple insulation
Input ↔ input	No
Effect with cross-polarity of inputs	No destruction, no high currents

[1)] at UC = Nominal value

1.7.2.3 Digital Outputs

The digital outputs of the CPU 72x have the following output switching:

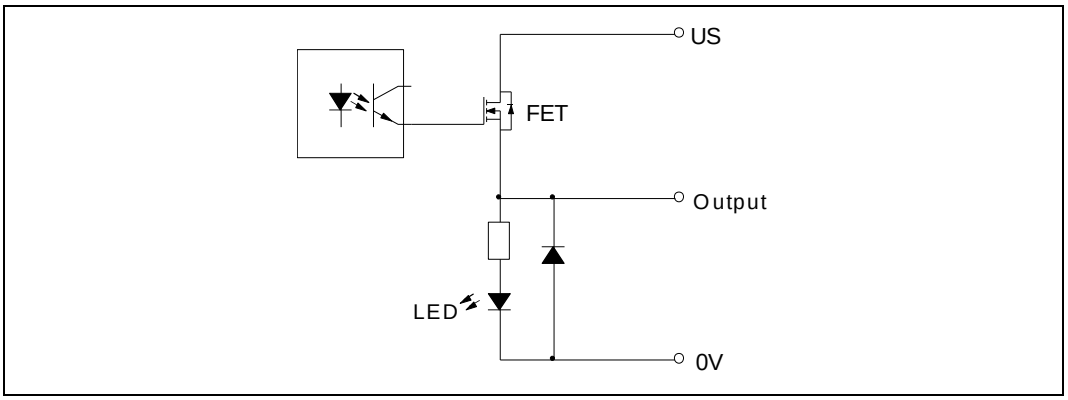


Fig.20: Connection diagram digital outputs

Legend:

Digital Outputs CPU 72x	**-T/LT**	**-TH/LTH**
Output type	FET, plus-switching	
Output display	LED orange, lights up with Signal = 1	
Power supply (US)		
Nominal value	24 Vdc	36 Vdc
Limits	16.8…30.0 Vdc	25.2…45.0 Vdc
Power supply display (US)	LED green	
Output voltage	≥ 23 Vdc	≥ 35 Vdc
Output current with Signal = 1 max.	0.5 A	
Short circuit current Is typ.	5 A, switch off time = 1.5 ms	
Switch on time after short circuit	5 s	
Short circuit display	LED ret	
Total loading [1)]	2 A // 4 A	
Minimum switching current	100 µA	
Limitation of inductive switch off voltage	Suppressor diode	
Output delay		
for Signal 0 → 1	600 µs	
for Signal 1 → 0	800 µs	
Switching frequency		
resistive load	100 Hz	
inductive load	2 Hz	
Signal level of outputs without load		
for Signal 0	max. 2 Vdc	
for Signal 1	16.8…30.0 Vdc	25.2…45.0 Vdc
Effect with overload	outputs are switched off	
Galvanic separation		
Output ↔ logic	Yes, simple insulation, opto-coupler	
Output ↔ output	No	
Test voltage	560 Vac, 800 Vdc to logic and earth	

[1)] 2 A at CPU 723-T — 4 A at CPU 725-LT/LTH / CPU 727-T/TH

1.8 Accessories: Flash Cassette FMC 701-T

The FMC 701-T flash cassette serves to store the user program or parameters. It has a memory capacity of 1 MB. As the time delay system can be copied onto the cassette with the user program, program swaps are possible over long distances.

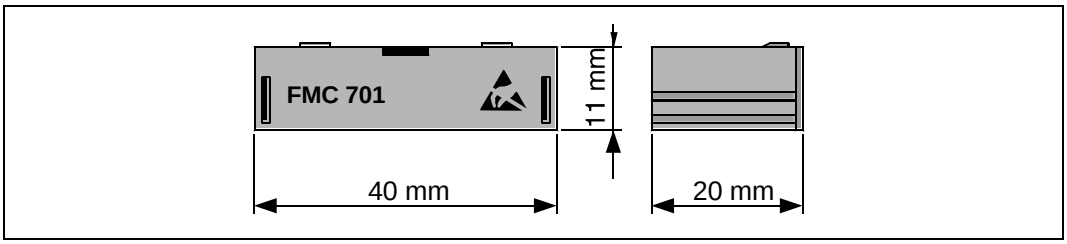


Fig.21: Dimensions flash cassette FMC 701-T

Procedure

To insert the memory cassette, please proceed as follows:

1. Switch off the power supply to the CPU and remove the cover with screwdriver no. 2.
2. + 3. Insert the memory cassette with the guide groove facing downwards and check that it is correctly seated.

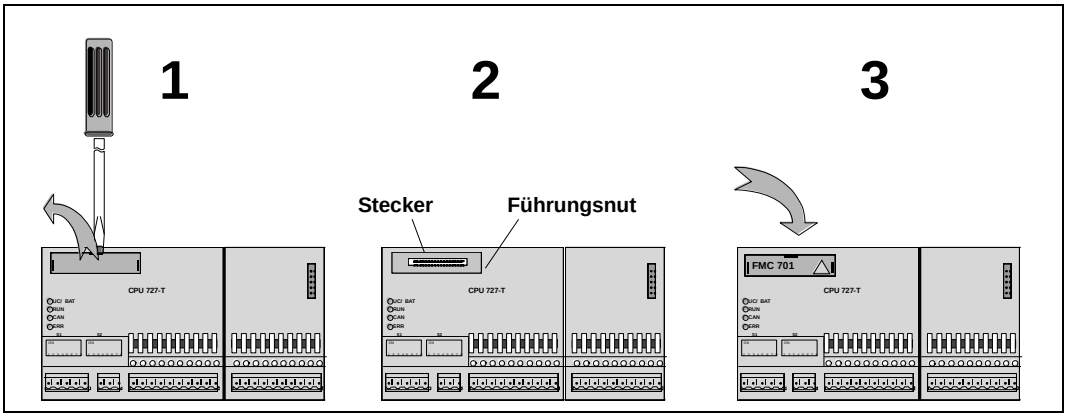


Fig.22: Mounting the flash cassette

IMPORTANT

The memory cassette must **not** be inserted or removed while the CPU is powered up. The cassette plug and the CPU must **not** be touched.

Note

- Please check the S2 DIP switch S2 so that the CPU starts up in the correct mode after the memory cassette has been inserted (see 1.5.1, pg.15).
- The procedure for programming the flash cassette is contained in the "System Manual MAS Software", chapter "MAS Programming", 3.4 Operating statuses and startup behavior.

1.8.1 Technical Data

Technical Data FMC 701-T	
Flash-EPROM	1MByte (256k x16)
Programming	Sector by sector
Usable with	CPU 723-T, CPU 727-T/TH
Article no.	44170232