8-1 High-speed Counter Board

8-1-1 Model

Name	Model	Specification
High-speed Counter Board	CQM1H-CTB41	Four pulse inputs Four external outputs of comparison result

8-1-2 Functions

The High-speed Counter Board is an Inner Board that handles four pulse inputs.

High-speed Counter Pulse Inputs 1 to 4
The High-speed Counter Board counts high-speed pulses from 50 to 500 kHz entering through ports 1 to 4, and performs tasks according to the number of pulses counted.

Input Modes
The following three Input Modes are available:

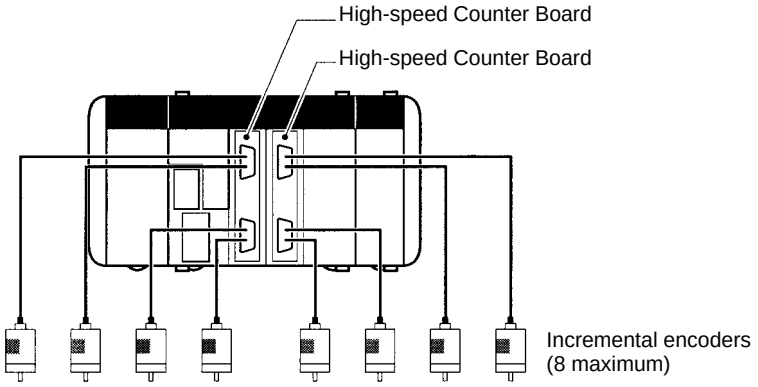
- Differential Phase Mode (1x/2x/4x)
- Up/Down Mode
- Pulse/Direction Mode

Comparison Operation
When the PV (present value) of the high-speed counter matches a specified target value or lies within a specified range, the bit pattern specified in the comparison table is stored in internal output bits and external output bits. A bit pattern can be set for each comparison result, and the external output bits can be output through an external output terminal as described below.

External Outputs
Up to four external outputs can be produced when either the target value is matched or a range comparison condition is satisfied.

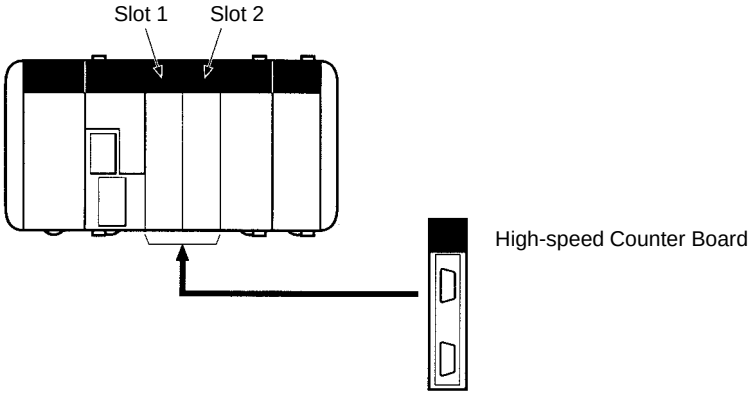
Note The High-speed Counter Board does not provide high-speed counter interrupts. It simply compares the PV to target values or comparison ranges, and produces internal and external bit outputs.

8-1-3 Example System Configuration



8-1-4 Applicable Inner Board Slots

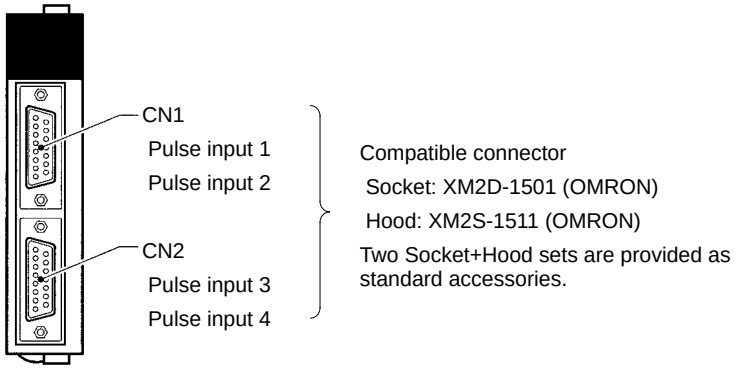
The High-speed Counter Board can be installed in either slot 1 (left slot) or slot 2 (right slot) of the CQM1H-CPU51/61 CPU Unit. Both slots can be used at the same time.



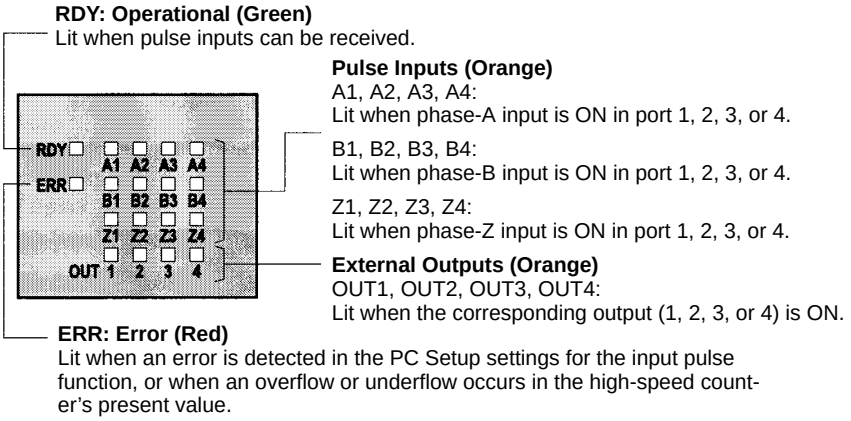
8-1-5 Names and Functions

One High-speed Counter Board provides two connectors that accept high-speed pulse inputs. CN1 is used for inputs 1 and 2, and CN2 is used for inputs 3 and 4.

CQM1H-CTB41 High-speed Counter Board

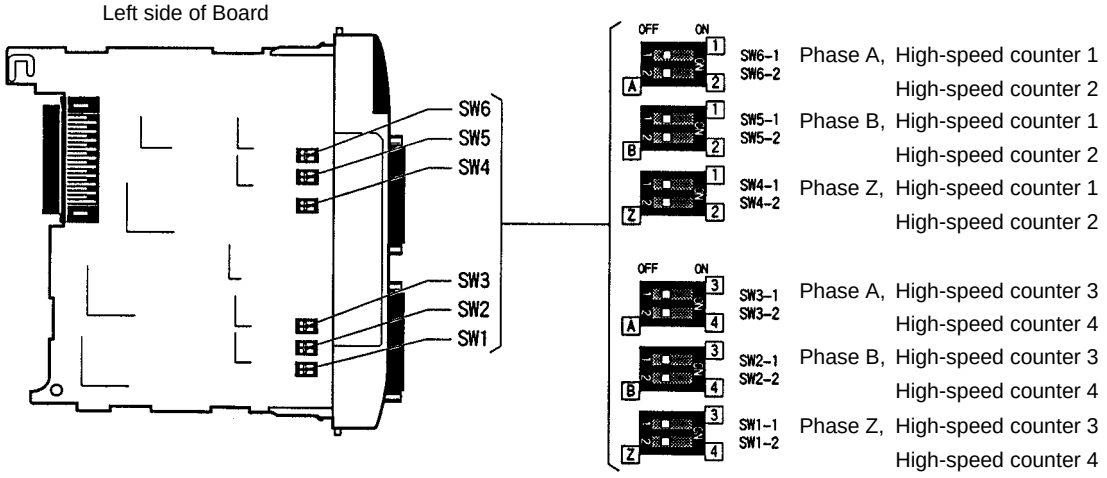


LED Indicators



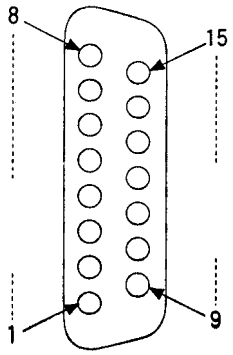
Input Voltage Level Switches

Counter 1	Counter 2	Counter 3	Counter 4	Status	Setting	
SW6-1	SW6-2	SW3-1	SW3-2	ON	Counter input: Input voltage A	Line driver level
				OFF		24-V DC level (default)
SW5-1	SW5-2	SW2-1	SW2-2	ON	Counter input: Input voltage B	Line driver level
				OFF		24-V DC level (default)
SW4-1	SW4-2	SW1-1	SW1-2	ON	Counter input: Input voltage Z	Line driver level
				OFF		24-V DC level (default)

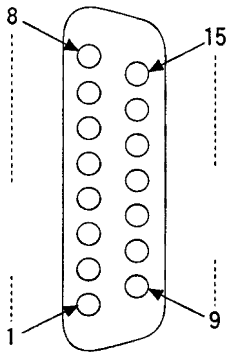


8-1-6 Pin Arrangement of Connectors CN1 and CN2

CN1: Pulse Input 1 and 2

Pin arrangement	Pin No.	Name	Function
	1	2OUT	External output 2
	2	1OUT	External output 1
	3	1Z–	Counter 1 input: Z –
	4	1Z+	Counter 1 input: Z +
	5	1B–	Counter 1 input: B –
	6	1B+	Counter 1 input: B +
	7	1A–	Counter 1 input: A –
	8	1A+	Counter 1 input: A +
	9	+DC	Power supply for external outputs 1 to 4: 5 to 24 V DC
	10	2Z–	Counter 2 input: Z –
	11	2Z+	Counter 2 input: Z +
	12	2B–	Counter 2 input: B –
	13	2B+	Counter 2 input: B +
	14	2A–	Counter 2 input: A –
	15	2A+	Counter 2 input: A +
	Hood	NC	Not used.

CN2: Pulse Input 3 and 4

Pin arrangement	Pin No.	Name	Function
	1	3Z–	Counter 3 input: Z –
	2	3Z+	Counter 3 input: Z +
	3	3B–	Counter 3 input: B –
	4	3B+	Counter 3 input: B +
	5	3A–	Counter 3 input: A –
	6	3A+	Counter 3 input: A –
	7	4OUT	External output 4
	8	3OUT	External output 3
	9	4Z–	Counter 4 input: Z –
	10	4Z+	Counter 4 input: Z +
	11	4B–	Counter 4 input: B –
	12	4B+	Counter 4 input: B +
	13	4A–	Counter 4 input: A –
	14	4A+	Counter 4 input: A +
	15	–DC	Power supply for external outputs 1 to 4: 0 V
	Hood	NC	Not used.

Note Refer to *Appendix A Preparing Cables for Inner Boards* for information about using a compatible connector (XM2D-1501 Socket with XM2S-1511 Hood) to construct a cable.

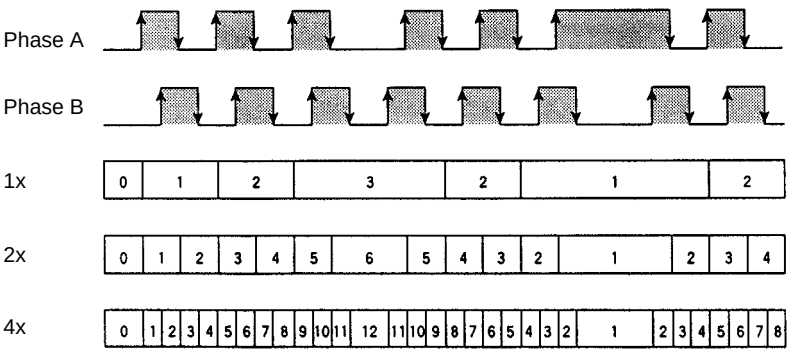
8-1-7 Wiring Examples

Pulse Input Connections Connect the encoder outputs to CN1 and CN2 as shown below according to the port's Input Mode.

CN1 pins		CN2 pins		Signal name	Encoder output		
Port 1	Port 2	Port 3	Port 4		Differential Phase Mode	Pulse/Direction Mode	Up/Down Mode
8 (7)	15 (14)	6 (5)	14 (13)	Encoder input A	Encoder phase A input	Pulse input	Increment pulse input
6 (5)	13 (12)	4 (3)	12 (11)	Encoder input B	Encoder phase B input	Directional signal input	Decrement pulse input

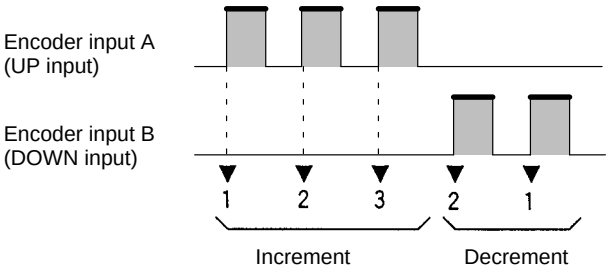
Note Pin numbers for negative pins are given in parentheses.

Differential Phase Mode

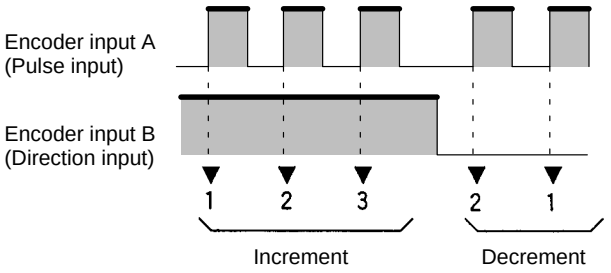


Phase A	Phase B	1x	2x	4x
↑	L	Count up	Count up	Count up
H	↑	---	---	Count up
↓	H	---	Count up	Count up
L	↓	---	---	Count up
L	↑	---	---	Count down
↑	H	---	Count down	Count down
H	↓	---	---	Count down
↓	L	Count down	Count down	Count down

Up/Down Mode



Pulse/Direction Mode

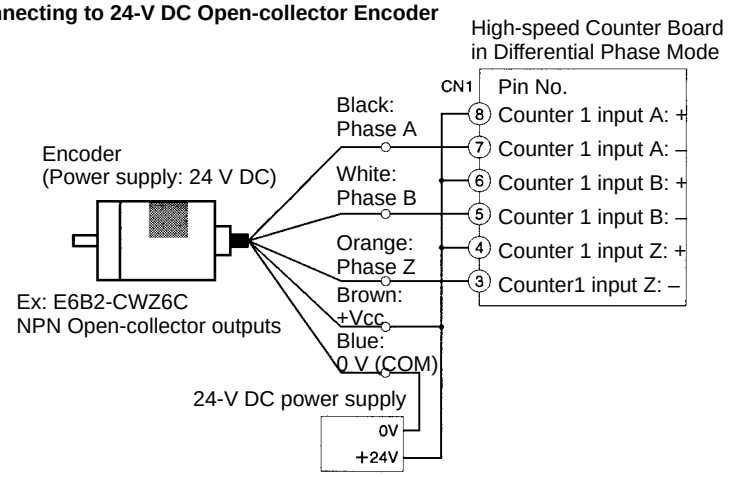


Note The function of encoder inputs A and B in Pulse/Direction Mode and Up/Down Mode differs from the Pulse I/O Board (CQM1H-PLB21).

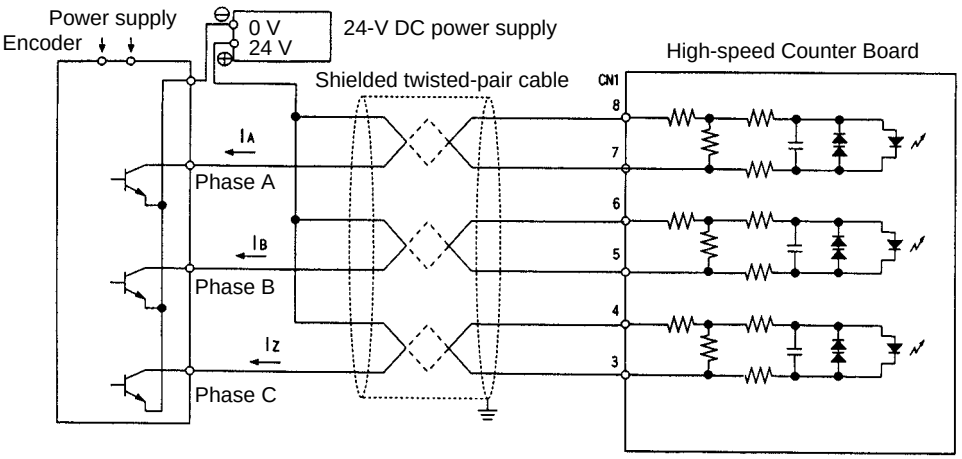
Wiring Examples

The following diagrams show a connection to an encoder possessing phases A, B, and Z.

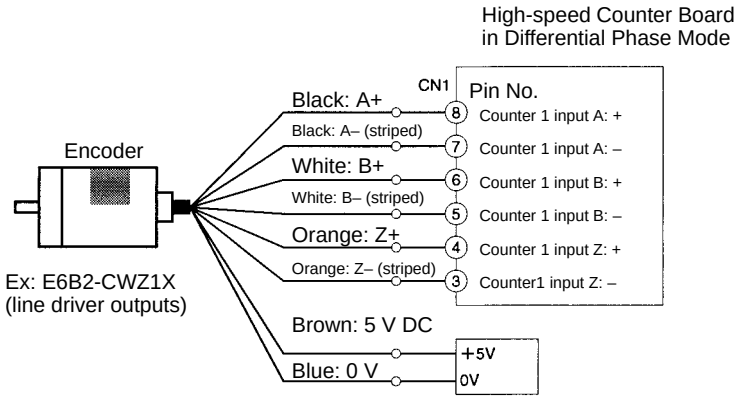
Connecting to 24-V DC Open-collector Encoder

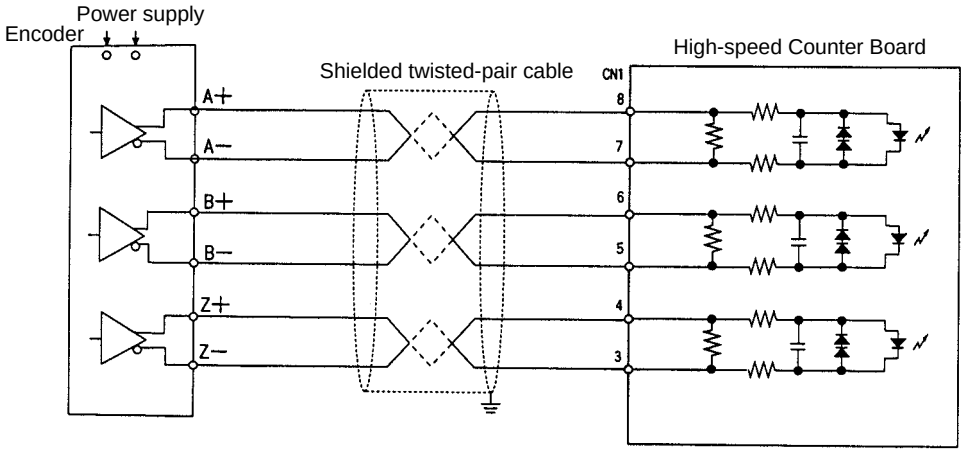


(Do not share the power supply with other I/O.)



Connecting to an Encoder with a Line-driver Output (Am26LS31)





External Output Connections

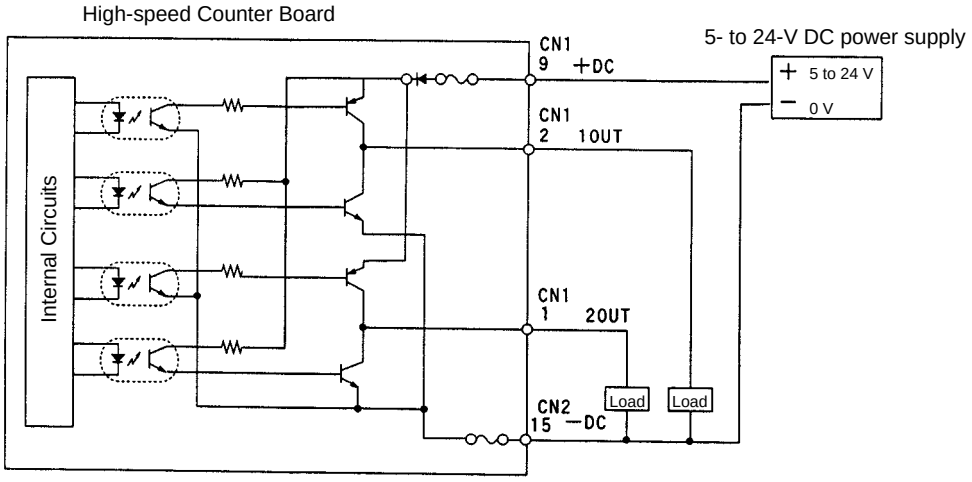
The comparison results of high-speed counters 1 to 4 generate four external bit patterns. An OR is taken of corresponding bits in these 4-bit patterns, and the result is then output on external outputs 1 to 4. The bit patterns are set by the user when programming the comparison operation.

Connector	Pin no.	Name	Content
CN1	2	1OUT	External output 1
	1	2OUT	External output 2
	9	+DC	Power supply for external outputs 1 to 4: 24 V DC
CN2	8	3OUT	External output 3
	7	4OUT	External output 4
	15	–DC	Power supply for external outputs 1 to 4: 0 V

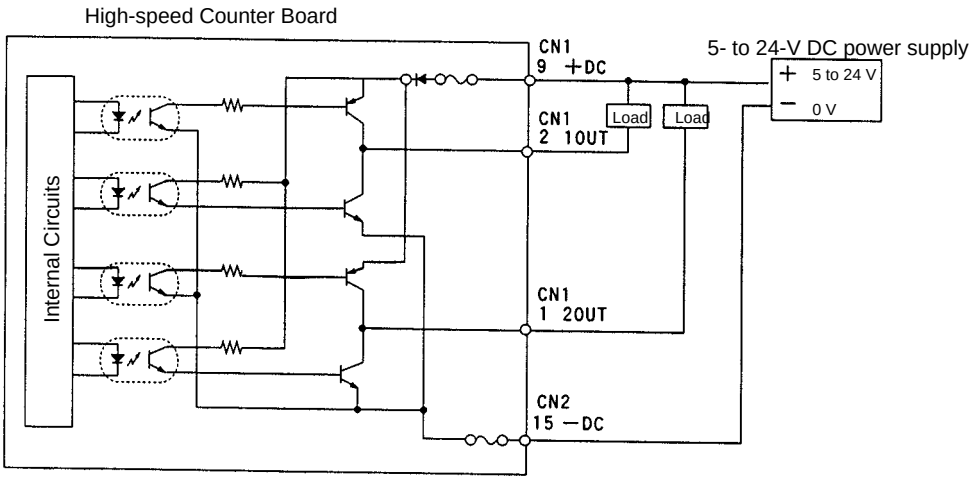
Note Switching between sourcing (PNP) outputs and sinking (NPN) outputs is accomplished using the PC Setup (DM 6602, DM 6611).

Example External Output Lines

Sourcing (PNP) Output



Sinking (NPN) Outputs



8-1-8 Specifications

Item	Specifications
Name	High-speed Counter Board
Model number	CQM1H-CTB41
Applicable CPU Units	CQM1H-CPU51/61
Unit classificatiion	CQM1H-series Inner Board
Mounting locations and number of Boards	Maximum of two Boards can be mounted simultaneously in slots 1 and 2.
Pulse inputs	4 inputs (Refer to *High-speed Counter Specifications* below for details.)
External outputs	4 outputs (Refer to *External Output Specifications* below for details.)
Settings	Input voltage level switch
Indicators	Front: 18 LEDs 1 each of Ready (RDY) and Error (ERR) 4 each of phase A (A□), phase B (B□), phase Z (Z□), and external output (OUT□)
Front connections	Connectors CN1 and CN2 (Compatible connectors: Sockets & Hoods provided as standard accessories.)
Current consumption (Supplied from Power Supply Unit)	5 V DC 400 mA max.
Dimensions	25 × 110 × 107 mm (W × H × D)
Weight	90 g max.
Standard accessories	Sockets: XM2D-1501 (OMRON) x 2 Hoods: XM2S-1511 (OMRON) x 2

High-speed Counter Specifications

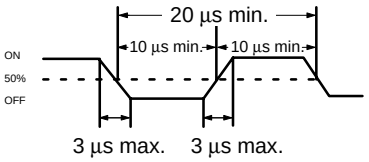
Counter Specifications

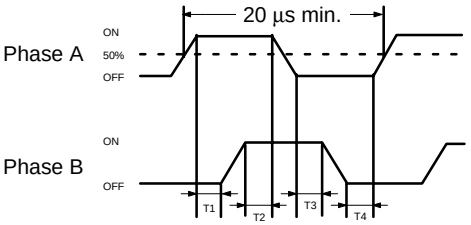
Item					Specifications		
Number of counters					4 counters (ports)		
Input Modes (Set in the PC Setup.)					Differential Phase Inputs	Up/Down Pulse Inputs	Pulse/Direction Inputs
Input pin No.	Port 1	Port 2	Port 3	Port 4	---		
	8 (7)	15 (14)	6 (5)	14 (13)	Phase-A input	Increment pulse input	Pulse input
	6 (5)	13 (12)	4 (3)	12 (11)	Phase-B input	Decrement pulse input	Direction input
	4 (3)	11 (10)	2 (1)	10 (9)	Phase-Z input	Reset input	Reset input
Input method					Switching between inputs using phase difference multiples of 1x, 2x, or 4x. (Set in the PC Setup.)	2, single-phase inputs	Single-phase pulse and direction inputs
Count frequency (Set for each port in the PC Setup.)					25 kHz (default) or 250 kHz	50 kHz (default) or 500 kHz	50 kHz (default) or 500 kHz
Count value					Linear Mode: –8388608 to 8388607 BCD, F8000000 to 07FFFFFF Hex Ring Mode: 00000000 to 08388607 BCD, 00000000 to 07FFFFFF Hex (Maximum value can be set to within the range 1 to 08388607 BCD, 1 to 07FFFFFF Hex with CTBL(63).)		

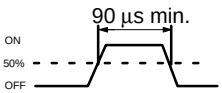
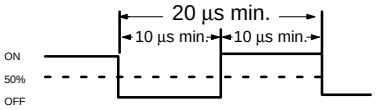
Item		Specifications
Storage location of counter PV		When mounted in slot 1: Port 1: IR 201 (leftmost digits) and IR 200 (rightmost digits) Port 2: IR 203 (leftmost digits) and IR 202 (rightmost digits) Port 3: IR 205 (leftmost digits) and IR 204 (rightmost digits) Port 4: IR 207 (leftmost digits) and IR 206 (rightmost digits) When mounted in slot 2: Port 1: IR 233 (leftmost digits) and IR 232 (rightmost digits) Port 2: IR 235 (leftmost digits) and IR 234 (rightmost digits) Port 3: IR 237 (leftmost digits) and IR 236 (rightmost digits) Port 4: IR 239 (leftmost digits) and IR 238 (rightmost digits) Data format: 8-digit BCD or 8-digit Hex (Set in the PC Setup: Bits 00 to 03 of DM 6602/DM 6611.) Linear Mode: F8388608 to 8388607 BCD (Leftmost digit is F Hex for negative numbers.) F8000000 to 07FFFFFF Hex Ring Mode: 00000000 to 08388607 BCD 00000000 to 07FFFFFF Hex
Control method	Target value match	Up to 48 target values and external/internal output bit patterns registered.
	Range comparison	Up to 16 upper limits, lower limits, and external/internal output bit patterns registered.
Counter reset method		**Phase-Z Signal + Software Reset** A counter is reset on the first phase-Z signal input after its Reset Bit (see below) is turned ON. **Software Reset** A counter is reset when its Reset Bit (see below) is turned ON. Reset Bits IR 21200 to IR 21203 (For ports 1 to 4 in slot 1) AR 0500 to AR 0503 (For ports 1 to 4 in slot 2)

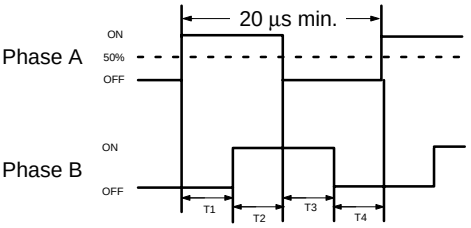
Pulse Input Specifications

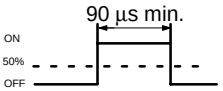
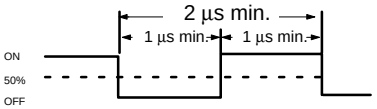
Item	Specifications			
Number of pulse inputs	4 inputs (Ports 1 to 4 = High-speed counters 1 to 4)			
Signals	Encoder inputs A and B; pulse input Z			
Input voltage	Switched by means of input voltage switch on the Board (Specified separately for phases A, B, and Z.)			
	24 V DC±10%		RS-422A line driver (AM26LS31 or equivalent)	
	Phase A and B	Phase Z	Phase A and B	Phase Z
Input current	5 mA typical	8 mA typical	10 mA typical	13 mA typical
ON voltage	19.6 V DC min.	18.6 V DC min.	---	---
OFF voltage	4.0 V DC min.	4.0 V DC min.	---	---

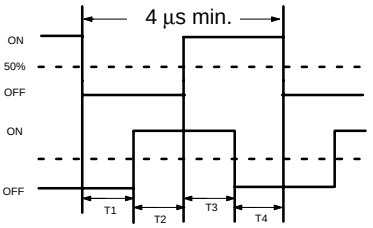
<table>
<tr><th>Item</th><th colspan="2">Specifications</th></tr>
<tr><td colspan="3">Min. response pulse</td></tr>
<tr><td>50 kHz setting</td><td>Encoder inputs A and B
Waveform of encoder inputs A and B
Input rise/fall time: 3 μs max.
50 kHz, pulse with duty factor of 50%
 

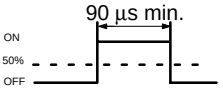
3 μs max. 3 μs max.
Relationship between phases A and B when phase differential input is used.
T1, T2, T3, T4: 4.5 μs min.
At least 4.5 μs must be provided to allow Phase A ↔ Phase B change.
 

Waveform of encoder input Z/Sensor input
Pulse width must be 90 μs min.
 
</td><td>Encoder inputs A and B
Waveform of + terminal
50 kHz, pulse with duty factor of 50%
 

Relationship between phases A and B when phase differential input is used.
T1, T2, T3, T4: 4.5 μs min.
At least 4.5 μs must be provided to allow Phase A ↔ Phase B change.
 

Waveform of encoder input Z/Sensor input
Pulse width must be 90 μs min.
 
</td></tr>
<tr><td>500 kHz setting</td><td>The counting operation at 500 kHz is not reliable.</td><td>Encoder inputs A and B
Waveform of + terminal
500 kHz, pulse with duty factor of 50%
 

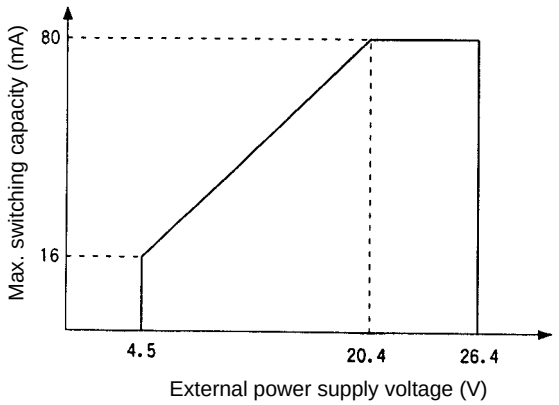
Relationship between phases A and B when phase differential input is used.
T1, T2, T3, T4: 1.0 μs min.
At least 1.0 μs must be provided to allow Phase A ↔ Phase B change.
 

Waveform of encoder input Z/Sensor input
Pulse width must be 90 μs min.
 
</td></tr>
</table>

External Output Specifications

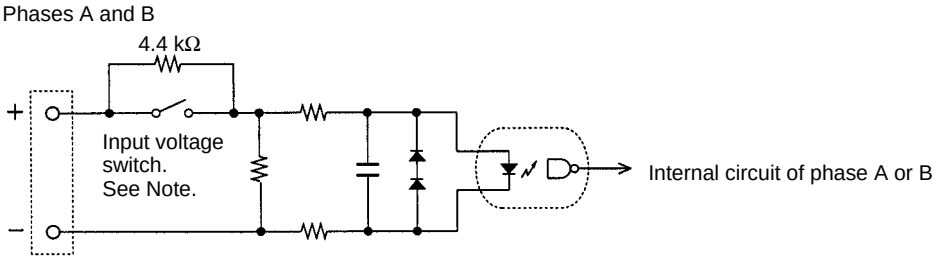
Item	Specifications
Number of external outputs	4 transistor outputs (Four outputs set together for sinking or sourcing outputs: Set in PC Setup)
Function	The target comparison or range comparison results of high-speed counters 1 to 4 output four user-defined 4-bit external bit patterns. An OR is taken of corresponding bits in these bit patterns, and the result is output on external outputs 1 to 4. **Note** External outputs 1 to 4 can be turned ON using IR 21300 to IR 21303 and AR 0600 to AR 0603.
External power supply	5 to 24 V DC±10%
Switching capacity	16 mA/4.5 V DC to 80 mA/26.4 V (see note)
Leakage current	0.1 mA max.
Residual voltage	0.8 V max.
Response for target matching	0.1 ms (This is the time required from completing target comparison until the external outputs are turned ON or OFF. The response time listed below must also be added.)
Response time	ON response: 0.1 ms max.; OFF response: 0.4 ms max.

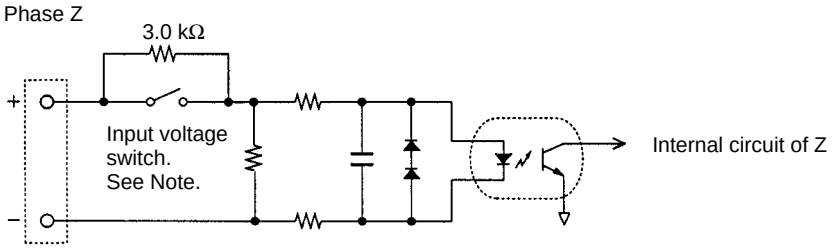
Note The switching capacity is shown below.



8-1-9 Internal Circuits

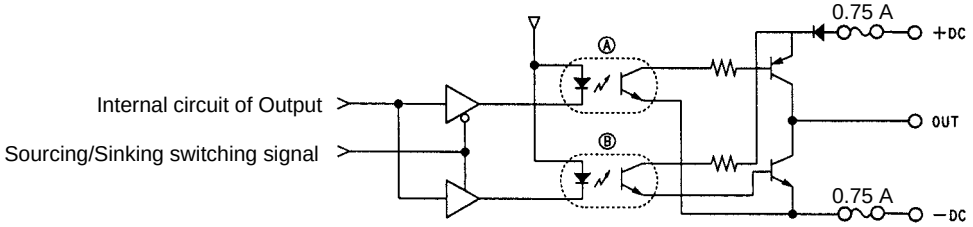
Pulse Inputs





Note ON: Line driver input
OFF: 24-V DC input

External Outputs



Note In the above figure, A is active when sourcing outputs are set, and B is active when sinking outputs are set.

8-2 Pulse I/O Board

8-2-1 Model

Name	Model	Specifications
Pulse I/O Board	CQM1H-PLB21	Two pulse input points and two pulse output points

8-2-2 Function

The Pulse I/O Board is an Inner Board that supports two pulse inputs and two pulse outputs.

Pulse Inputs 1 and 2

Pulse inputs 1 and 2 can be used as high-speed counters to count pulses input at either 50 kHz (signal phase) or 25 kHz (differential phase). Interrupt processing can be performed based on the present values (PV) of the counters.

Input Mode

The following three Input Modes are available:

- Differential Phase Mode (4x)

2-1-6 Specifications

Instructions

Instruction	Meaning
CTBL(63)	Used to register target or range comparison tables or used to start comparisons for previously registered comparison tables. A table can be registered and comparison started with separate instructions or the same instruction.
INI(61)	Used to start or stop comparison using registered comparison table or used to change the PV of a high-speed counter.
PRV(62)	Used to read the PV or status of a high-speed counter.

Related Control Bits, Flags, and Status Information

Word		Bits	Name		Function
Slot 1	Slot 2				
IR 200	IR 232	00 to 15	Counter 1	PV (rightmost four digits)	The PV of the high-speed counter on each port of the High-speed Counter Board is stored after each cycle. **Note** The form in which data is stored (BCD or hexadecimal) can be specified in the PC Setup (DM 6602 and DM 6611).
IR 201	IR 233	00 to 15		PV (leftmost four digits)	
IR 202	IR 234	00 to 15	Counter 2	PV (rightmost four digits)	
IR 203	IR 235	00 to 15		PV (leftmost four digits)	
IR 204	IR 236	00 to 15	Counter 3	PV (rightmost four digits)	
IR 205	IR 237	00 to 15		PV (leftmost four digits)	
IR 206	IR 238	00 to 15	Counter 4	PV (rightmost four digits)	
IR 207	IR 239	00 to 15		PV (leftmost four digits)	
IR 208: Counter 1 IR 209: Counter 2 IR 210: Counter 3 IR 211: Counter 4	IR 240: Counter 1 IR 241: Counter 2 IR 242: Counter 3 IR 243: Counter 4	00 to 07	Comparison Results: Internal Output Bits 00 to 07		Contains the bit pattern specified by operand in CTBL(63) when a condition is satisfied.
		08 to 11	Comparison Results: Bits for External Outputs 1 to 4		Contains the bit pattern specified by operand in CTBL(63) when a condition is satisfied.
		12	Counter Operating Flag		0: Stopped 1: Operating
		13	Comparison Flag		Indicates whether or not a comparison is in progress. 0: Stopped 1: Operating
		14	PV Overflow/Underflow Flag		Indicates whether or not an overflow or underflow has occurred. 0: Normal 1: Overflow or underflow has occurred
		15	SV Error Flag		0: Normal 1: Setting error

Word		Bits	Name	Function
Slot 1	Slot 2			
IR 212	AR 05	00	High-speed counter 1 Reset Bit	Phase Z and software reset 0: Counter not reset on phase Z 1: Counter reset on phase Z Software reset only 0: Counter not reset 0→1: Counter reset
		01	High-speed counter 2 Reset Bit	
		02	High-speed counter 3 Reset Bit	
		03	High-speed counter 4 Reset Bit	
		08	High-speed Counter 1 Comparison Start Bit	0 → 1: Comparison starts 1 → 0: Comparison stops
		09	High-speed Counter 2 Comparison Start Bit	
		10	High-speed Counter 3 Comparison Start Bit	
		11	High-speed Counter 4 Comparison Start Bit	
		12	High-speed Counter 1 Stop Bit	0: Operation continues 1: Operation stops
		13	High-speed Counter 2 Stop Bit	
		14	High-speed Counter 3 Stop Bit	
		15	High-speed Counter 4 Stop Bit	
IR 213	AR 06	00	External Output 1 Force-set Bit	0: No effect on output status 1: Forces output ON
		01	External Output 2 Force-set Bit	
		02	External Output 3 Force-set Bit	
		03	External Output 4 Force-set Bit	
		04	External Output Force-set Enable Bit	0: Force-setting of outputs 1 to 4 disabled 1: Force-setting of outputs 1 to 4 enabled
SR 254		15	Inner Board Error Flag	0: No error 1: Error Turns ON when an error occurs in an Inner Board mounted in slot 1 or slot 2. The error code for slot 1 is stored in AR 0400 to AR 0407 and the error code for slot 2 is stored in AR 0408 to AR 0415.
AR 04		00 to 07	Error code for Inner Board in slot 1	00 Hex: Normal 01 or 02 Hex: Hardware error 03 Hex: PC Setup error
		08 to 15	Error code for Inner Board in slot 2	

Related PC Setup Settings

Word		Bits	Function	When setting is read
Slot 1	Slot 2			
DM 6602	DM 6611	00 to 03	Data format in which PVs of high-speed counters 1 to 4 are stored 0: Eight-digit hexadecimal (BIN) 1: Eight-digit BCD	When power is turned ON.
		04 to 07	Not used.	
		08 to 11	Sourcing/Sinking setting for external outputs 1 to 4 0: Sourcing (PNP) 1: Sinking (NPN)	
		12 to 15	Not used.	
DM 6640	DM 6643	00 to 03	Input Mode for high-speed counter 1 0 Hex: 1x Differential phase input 1 Hex: 2x Differential phase input 2 Hex: 4x Differential phase input 3 Hex: Up/Down pulse input 4 Hex: Pulse/Direction input	When operation starts.
		04 to 07	Count frequency, Numeric Range Mode and counter reset method of high-speed counter 1. Refer to the following table.	
		08 to 11	Input Mode of high-speed counter 2 (Refer to the explanation given above for high-speed counter 1.)	
		12 to 15	Count frequency, Numeric Range Mode, and counter reset method of high-speed counter 2 (Refer to the explanation given above for high-speed counter 1.)	
DM 6641	DM 6644	00 to 03	Input Mode of high-speed counter 3 (Refer to the explanation given above for high-speed counter 1.)	
		04 to 07	Count frequency, Numeric Range Mode, and counter reset method of high-speed counter 3 (Refer to the explanation given above for high-speed counter 1.)	
		08 to 11	Input Mode of high-speed counter 4 (Refer to the explanation given above for high-speed counter 1.)	
		12 to 15	Count frequency, Numeric Range Mode, and counter reset method of high-speed counter 4 (Refer to the explanation given above for high-speed counter 1.)	

Count Frequency, Numeric Range Mode, and Counter Reset Method of High-speed Counters

Value	Count frequency	Numeric Range Mode	Counter reset method
0 Hex	50 KHz	Linear Mode	Phase Z + software reset
1 Hex			Software reset only
2 Hex		Ring Mode	Phase Z + software reset
3 Hex			Software reset only
4 Hex	500 KHz	Linear Mode	Phase Z + software reset
5 Hex			Software reset only
6 Hex		Ring Mode	Phase Z + software reset
7 Hex			Software reset only

2-1-7 High-speed Counters 1 to 4

The High-speed Counter Board counts pulse signals entering through ports 1 to 4 from rotary encoders and outputs internal/external output bit patterns according to the number of pulses counted. The four ports can be used independently. An outline of the processing performed by high-speed counters 1 to 4 is provided below.

Overview of Process

Input Signals and Input Modes

High-speed counters 1 to 4 can be set to different Input Modes in response to the type of signal input.

Differential Phase Mode (Counting Speed: 25 kHz or 250 kHz)

Two phase signals (phase A and phase B) with phase difference multiples of 1x, 2x, or 4x are used together with a phase-Z signal for inputs. The count is incremented or decremented according to differences in the two phase signals.

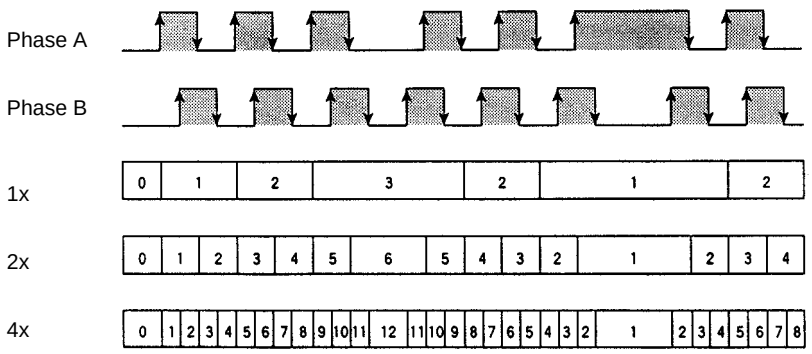
Up/Down Mode (Counting Speed: 50 kHz or 500 kHz)

Phase A is the incrementing pulse and phase B is the decrementing pulse. The counter increments or decrements according to the pulse that is detected.

Pulse/Direction Mode (Counting Speed: 50 kHz or 500 kHz)

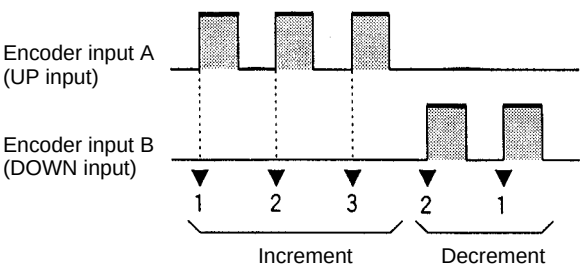
Phase A is the pulse signal and phase B is the direction signal. The counter increments when the phase-B signal is ON and decrements when it is OFF.

Differential Phase Mode

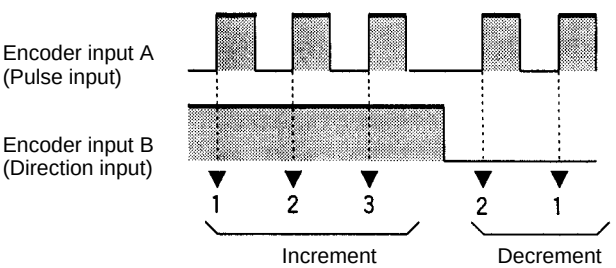


Phase A	Phase B	1x	2x	4x
↑	L	Increment	Increment	Increment
H	↑	---	---	Increment
↓	H	---	Increment	Increment
L	↓	---	---	Increment
L	↑	---	---	Decrement
↑	H	---	Decrement	Decrement
H	↓	---	---	Decrement
↓	L	Decrement	Decrement	Decrement

Up/Down Mode



Pulse/Direction Mode



Numeric Ranges

The values counted by high-speed counters 1 to 4 can be counted using the following two range settings:

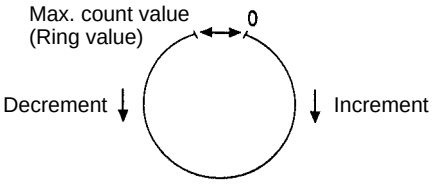
Ring Mode

In Ring Mode, the maximum value of a numerical range can be set using CTBL(63), and when the count is increment beyond this maximum value, it returns to zero. The count never becomes negative. Similarly, if the count is decremented from 0, it returns to the maximum value. The number of points on the ring is determined by setting the maximum value (i.e., the ring value) to a value between 1 and 8388607 BCD or between 1 and 7FFFFFFF Hex. When the maximum value is set to 8388607, the range will be 0 to 8388607 BCD.

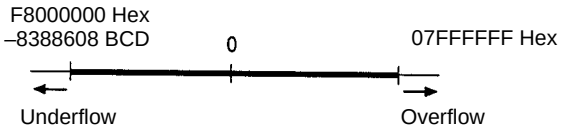
Linear Mode

In Linear Mode, the count range is always –8388608 to 8388607 BCD or F8000000 to 07FFFFFF Hex. If the count decrements below –8388608 BCD or F8000000 Hex, an underflow is generated, and if it increments above 8388607 BCD or 07FFFFFF Hex, an overflow is generated.

Ring Mode



Linear Mode



If an overflow occurs, the PV of the count will remain at 08388607 BCD or 07FFFFFF Hex, and if an underflow occurs, it will remain at F8388608 BCD or F8000000 Hex. In either case, counting and comparison will stop, but the comparison table will be retained in memory. The PV Overflow/Underflow Flag shown below will turn ON to indicate the underflow or overflow.

Counter	PV Overflow/Underflow Flag	
	Slot 1	Slot 2
High-speed counter 1	IR 20814	IR 24014
High-speed counter 2	IR 20914	IR 24114
High-speed counter 3	IR 21014	IR 24214
High-speed counter 4	IR 21114	IR 24314

When restarting the counting operation, use the reset methods given below to reset high-speed counters 1 and 2. (Counters will be reset automatically when program execution starts and finishes.)

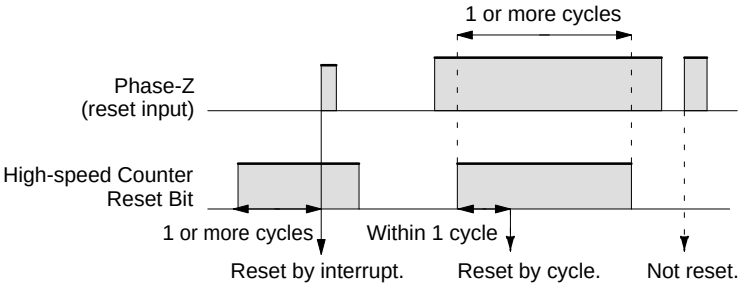
Reset Methods

The following two methods can be set to determine the timing at which the PV of the counter is reset (i.e., set to 0):

- Phase-Z signal + software reset
- Software reset

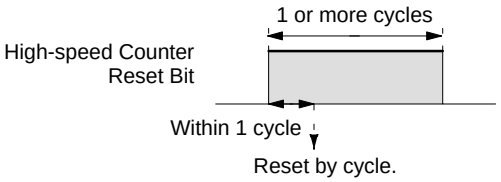
Phase-Z Signal (Reset Input) + Software Reset

The PV of the high-speed counter is reset in the first rising edge of the phase-Z signal after the corresponding High-speed Counter Reset Bit (see below) turns ON.



Software Reset

The PV is reset when the High-speed Counter Reset Bit turns ON. There are separate Reset Bits for each high-speed counter 1 to 4.



The Reset Bits of high-speed counters 1 to 4 are given in the following table.

Counter	Reset Bit	
	Slot 1	Slot 2
High-speed counter 1	IR 21200	AR 0500
High-speed counter 2	IR 21201	AR 0501
High-speed counter 3	IR 21202	AR 0502
High-speed counter 4	IR 21203	AR 0503

Reset Bits for high-speed counters 1 to 4 are refreshed only once each cycle. A Reset Bit must be ON for a minimum of 1 cycle to be read reliably.

Note The comparison table registration and comparison execution status will not be changed when the PV is reset. If a comparison was being executed before the reset, it will continue.

Checking Methods for High-speed Counter Interrupts

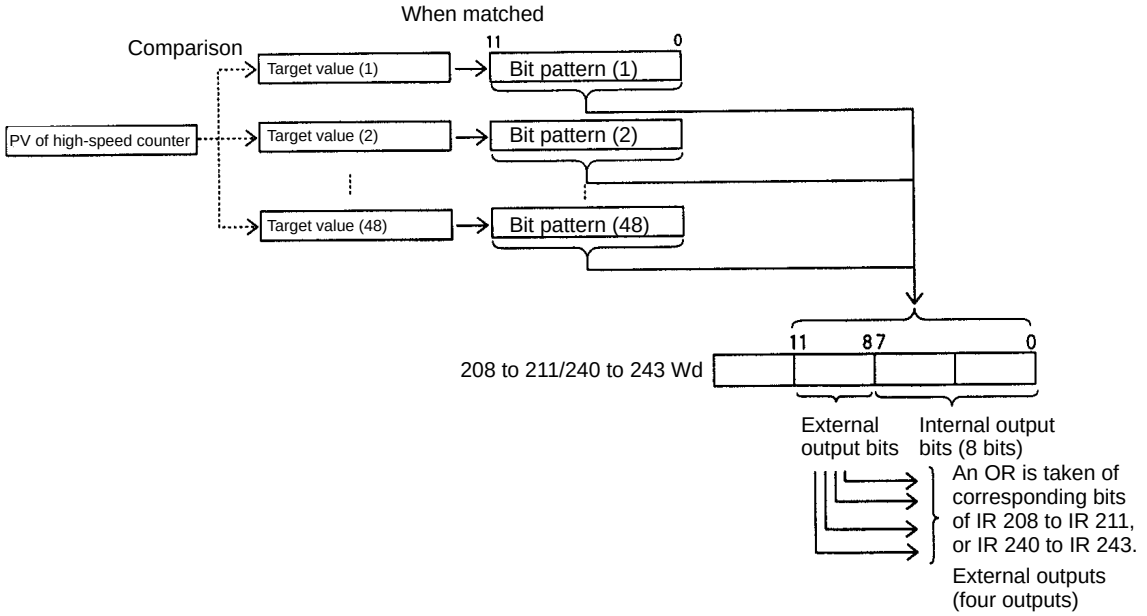
The following two methods are available to check the PV of high-speed counters 1 to 4. (These are the same methods as those used for built-in high-speed counter 0.)

- Target value method
- Range comparison method

Refer to page 31 for a description of each method.

For the target value method, a maximum of 48 target values can be registered in the comparison table. When the PV of the counter matches one of the 48 regis-

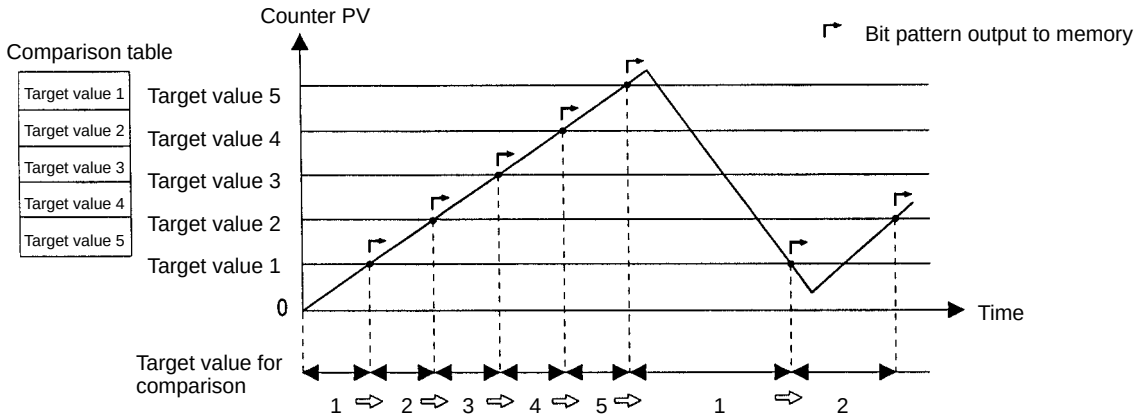
tered target values, the corresponding bit pattern (1 to 48) will be output to specific bits in memory.

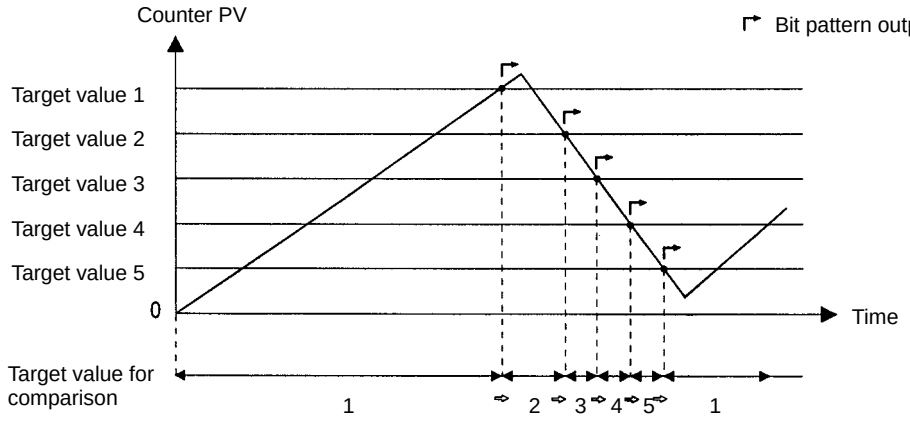


When using target values, comparison is made to each target value in the order of the comparison table until all values have been met, and then comparison will return to the first value in the table. With the High-speed Counter Board, it does not make any difference if the target value is reached as a result of incrementing or decrementing the PV.

Note With high-speed counter 0 in the CPU Unit or high-speed counter 1 or 2 on the Pulse I/O Board or Absolute Encoder Interface Board, the leftmost bit of the word containing the subroutine number in the comparison table determines if target values are valid for incrementing or for decrementing the PV.

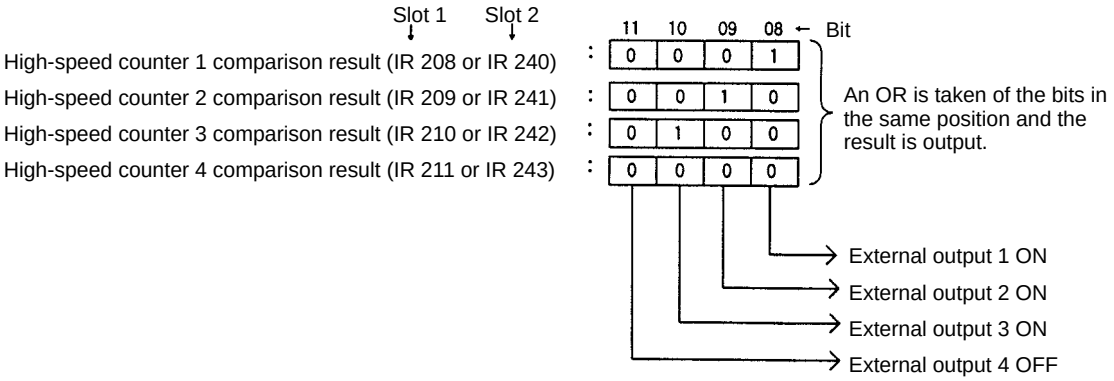
Examples of comparison table operation and bit pattern outputs are shown in the following diagrams.





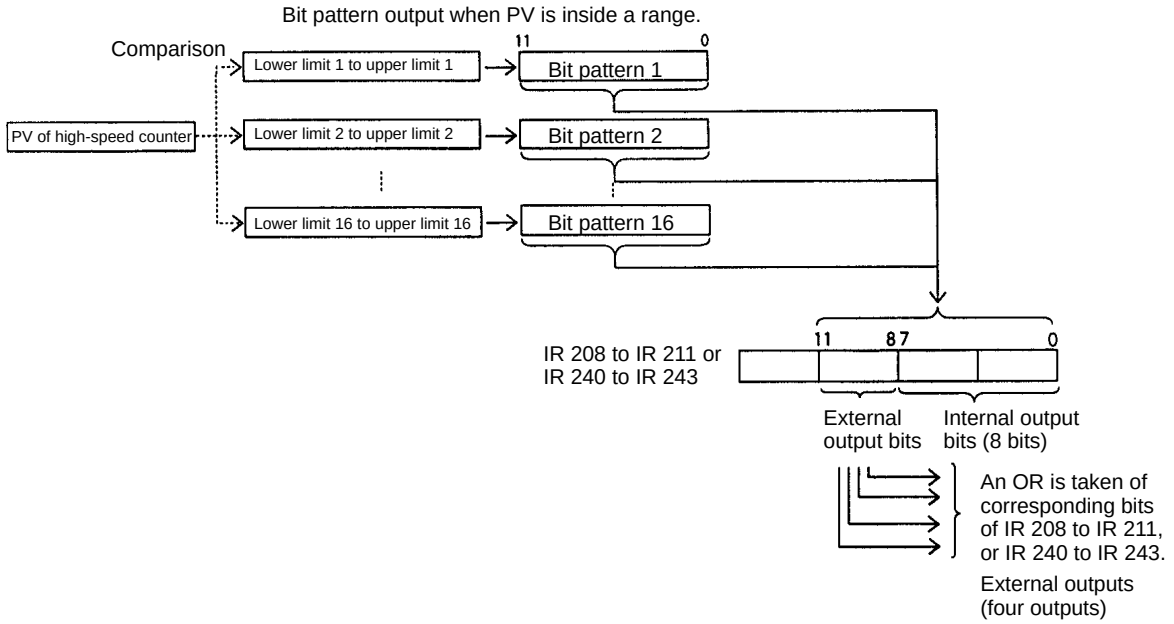
Comparison values 1 through 48 and bit patterns 1 through 48 are registered in the target value table. Of bits 00 to 11 of each of these bit patterns, bits 0 to 7 are stored as internal output bits, and bits 08 to 11 are stored as external output bits. As shown in the diagram below, the bits in the external bit pattern are used in an OR operation on the corresponding bits of high-speed counters 1 to 4, the results of which are then output as external outputs 1 to 4.

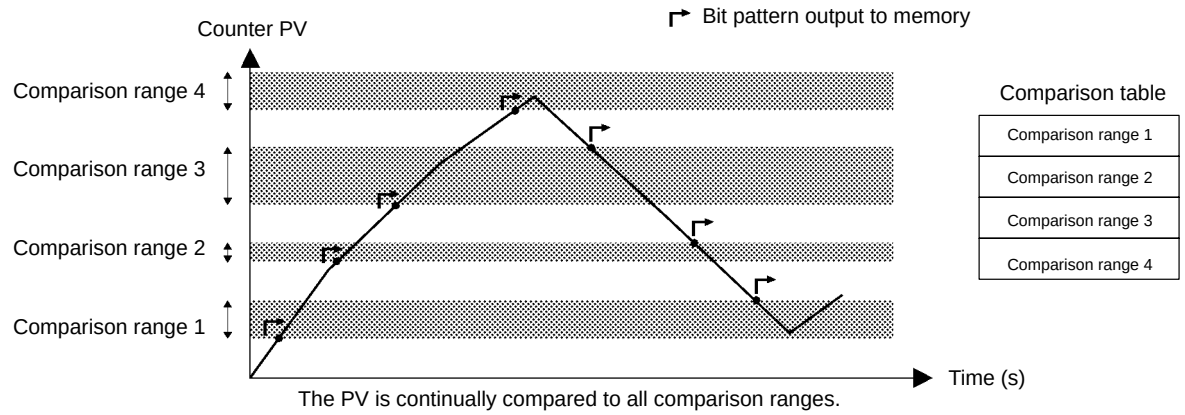
Example:



For the range comparison method, 16 comparison ranges are registered in the comparison table. When the PV of the counter first enters between the upper

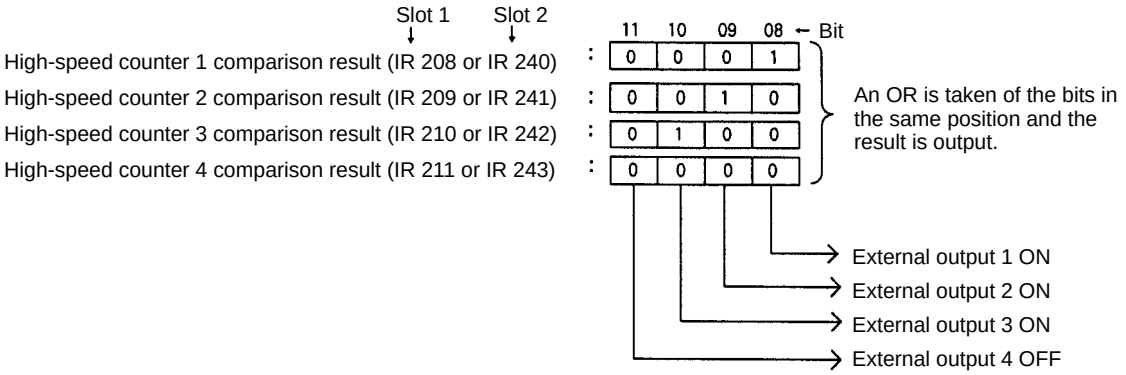
and lower limits of one of the ranges 1 to 16, the corresponding bit pattern (1 to 16) will be output once to specific bits in memory.





Lower and upper limits for ranges 1 through 16 and bit patterns 1 through 16 are registered in the range comparison table. Of bits 0 to 11 of each of these bit patterns, bits 0 to 7 are stored as internal output bits, and bits 8 to 11 are stored as external output bits. As shown in the diagram below, the bits in the external bit pattern are used in an OR operation on the corresponding bits of high-speed counters 1 to 4, the results of which are then output as external outputs 1 to 4.

Example:



External outputs 1 to 4 are controlled by ORs performed on corresponding bits (i.e., bits with the same bit number) in the comparison result bits 08 to 11 for high-speed counters 1 to 4. The user must determine which outputs should be turned ON for each possible comparison result and set the bit patterns so that the OR operations will produce the desired result.

Note Range Comparison Flags are supported by the built-in high-speed counter (high-speed counter 0) and the Pulse I/O Board for ranges1 to 8. These flags, however, are not supported by the High-speed Counter Board. The internal bit patterns must be used to produce the same type of output result.

Reading High-speed Counter Status

The following two methods can be used to read the status of high-speed counters 1 to 4:

- Using CPU Unit memory words
- Using PRV(62)

Using CPU Unit Memory Words

The memory area words and bits in the CPU Unit that indicate the status of high-speed counters 1 to 4 are given below.

Inner Board Error Codes

Word		Bits	Function	
Slot 1	Slot 2			
AR 04		00 to 07	Slot 1	The following 2-digit error codes are stored. 00 Hex: Normal 01 or 02 Hex: Hardware error 03 Hex: PC Setup error
		08 to 15	Slot 2	

Operating Status Words

High-speed counter	Word	
	Slot 1	Slot 2
High-speed counter 1	IR 208	IR 240
High-speed counter 2	IR 209	IR 241
High-speed counter 3	IR 210	IR 242
High-speed counter 4	IR 211	IR 243

The functions of the bits in each operating status word are as follows:

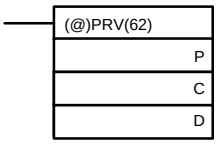
Bits	Function
00 to 07	Comparison Results: Internal Output Bits
08 to 11	Comparison Results: External Output Bits for Outputs 1 to 4 The result of an OR operation on bits in same bit positions for all the high-speed counters 1 to 4 will be output. (See note.)
12	Counter Operating Flag (0: Stopped; 1: Running)
13	Comparison Flag (0: Stopped; 1: Running)
14	PV Overflow/Underflow Flag (0: No; 1: Yes)
15	SV Error Flag (0: Normal; 1: Error)

Note The following table shows the relationship between external outputs 1 to 4 and Comparison Results External Output Bits.

High-speed counter	External output	Slot 1	Slot 2
Counter 1	External output 1	OR of bits 08 of IR 208 to IR 211	OR of bits 08 of IR 240 to IR 241
Counter 2	External output 2	OR of bits 09 of IR 208 to IR 211	OR of bits 09 of IR 240 to IR 241
Counter 3	External output 3	OR of bits 10 of IR 208 to IR 211	OR of bits 10 of IR 240 to IR 241
Counter 4	External output 4	OR of bits 11 of IR 208 to IR 211	OR of bits 11 of IR 240 to IR 241

Using PRV(62)

The status of high-speed counters 1 to 4 can be read using PRV(62) in the manner shown below.



P: Port specifier
C: 001
D: First destination word

High-speed counter	Value specified in P	
	Slot 1	Slot 2
High-speed counter 1	101	001
High-Speed counter 2	102	002
High-speed counter 3	103	003
High-speed counter 4	104	004

The meaning of the individual bits of D, in which the status of high-speed counters 1 to 4 is stored, is given in the following table.

Bits	Function
00 to 07	Comparison Results: Internal Output Bits
08 to 11	Comparison Results: External Output Bits for Outputs 1 to 4 The result of an OR operation on bits in same bit positions for all the high-speed counters 1 to 4 will be output. (See note.)
12	Counter Operating Flag (0: Stopped; 1: Running)
13	Comparison Flag (0: Stopped; 1: Running)
14	PV Overflow/Underflow Flag (0: No; 1: Yes)
15	SV Error Flag (0: Normal; 1: Error)

Procedure for Using High-speed Counters

Determine counting rate, Input Mode, reset method, Numeric Range Mode, form in which PV of high-speed counter data is stored, and external output method.

Counting rate: 50 kHz/500 kHz

Input Modes:
Differential Phase Mode; Pulse/Direction Mode; Up/Down Mode

Reset methods: Phase Z + software reset; software reset

Numeric Range Modes: Ring Mode or Linear Mode

Form in which PV of high-speed counter data is stored:
8-digit BCD or 8-digit hexadecimal

External output method:
Sourcing or Sinking switching of transistor output

↓

Set input voltages (switches on Board).

↓

Mount Board and wire inputs.

↓

PC Setup
(Slot 1: DM 6602, DM 6640, DM 6641
Slot 2: DM 6611, DM 6643, DM 6644)

Counting rate: 50 kHz/500 kHz

Input Modes:
Differential Phase Mode; Up/Down Mode; Pulse/Direction Mode

Reset methods:
Phase Z + software reset; software reset

Numeric Ranges: Ring Mode or Linear Mode

External output method:
Sourcing or Sinking switching of transistor output

Form in which PV of high-speed counter data is stored:
8-digit BCD; 8-digit hexadecimal

↓

Determine count check (comparison) method and internal/external bit patterns.

Count check methods: Target value or range comparison

Output bit patterns when conditions met:
Internal and external output bits

↓

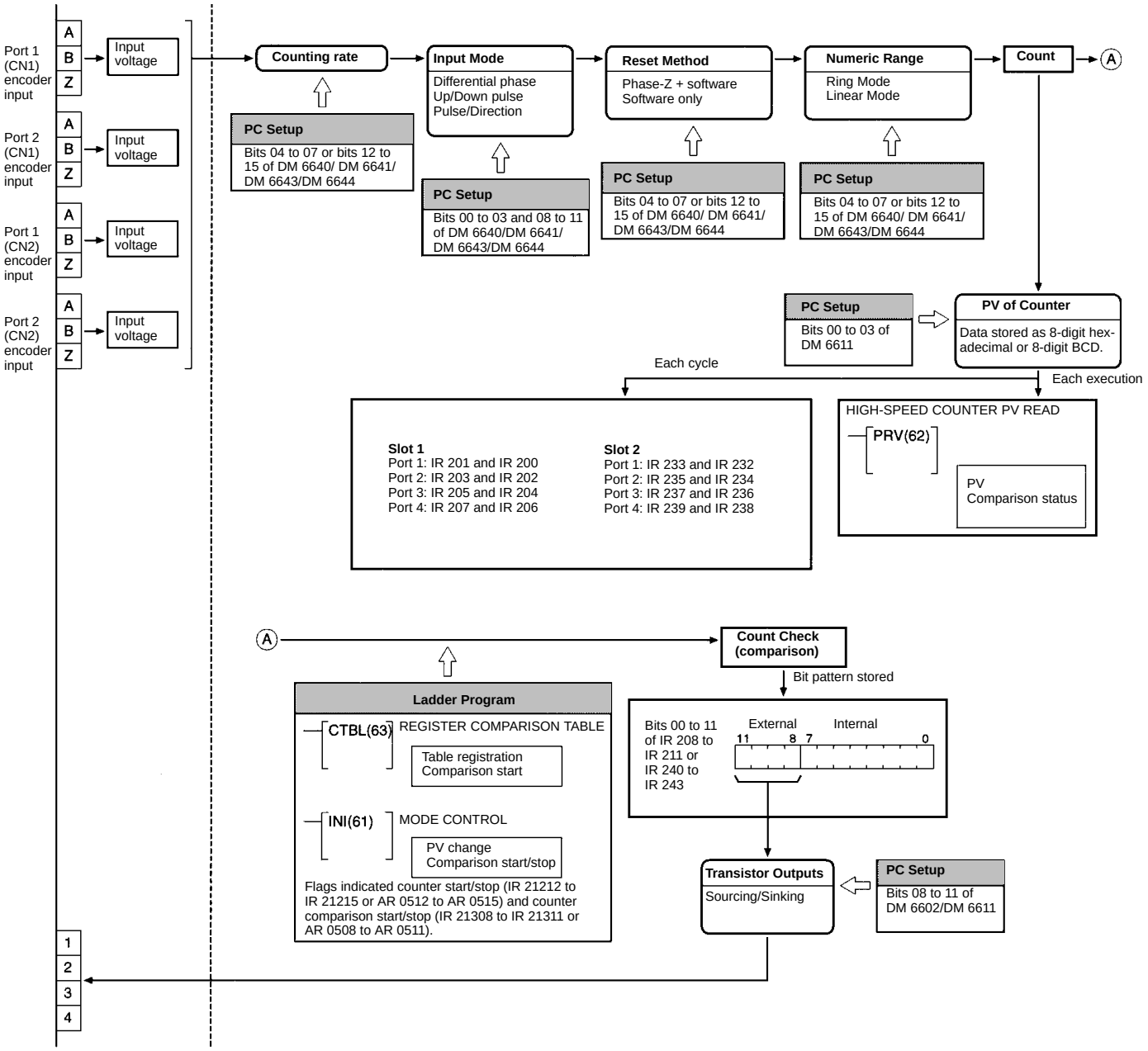
Ladder program

REGISTER COMPARISON TABLE (CTBL(63)):
Port specification; comparison table registration; comparison start

MODE CONTROL (INI(61)):
Port specification; PV change; comparison start

HIGH-SPEED COUNTER PV READ (PRV(62)):
Reading PV of high-speed counter and status of comparison.

High-speed Counter Function

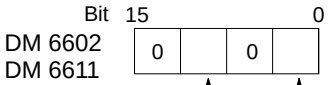


Preliminary PC Setup Settings

To use high-speed counters 1 to 4, make the following settings in PROGRAM mode.

Data Format and Sourcing/Sinking Setting for External Outputs

Slot 1: DM 6602
Slot 2: DM 6611



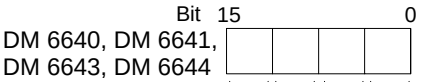
External Outputs 1 to 4 Transistor Selector
0 Hex: Sourcing (PNP)
1 Hex: Sinking (NPN)

High-speed Counters 1 to 4 PV Data Format
0 Hex: 8-digit hexadecimal (BIN)
1 Hex: 8-digit BCD

Default: 0000 (8-digit hexadecimal and sourcing (PNP))

Input Mode, Count Frequency, Numeric Range Mode, and Counter Reset Method

High-speed counter 1
Slot 1: Bits 00 to 07 of DM 6640 Slot 2: Bits 00 to 07 of DM 6643
High-speed counter 2
Slot 1: Bits 08 to 15 of DM 6640 Slot 2: Bits 08 to 15 of DM 6643
High-speed counter 3
Slot 1: Bits 00 to 07 of DM 6641 Slot 2: Bits 00 to 07 of DM 6644
High-speed counter 4
Slot 1: Bits 08 to 15 of DM 6641 Slot 2: Bits 08 to 15 of DM 6644



Count Frequency, Numeric Range Mode, and Counter Reset Method (See following table.)

High-speed Counter Input Mode
0 Hex: 1x Differential phase input
1 Hex: 2x Differential phase input
2 Hex: 4x Differential phase input
3 Hex: Up/Down pulse input
4 Hex: Pulse/Direction input

Default: 0000 (1x differential phase input, 50 kHz, Linear Mode, phase-Z + software reset)

Count Frequency, Numeric Range Mode, and Reset Method

Value	Count frequency	Numeric Range Mode	Counter reset method
0 Hex	50 KHz	Linear Mode	Phase Z + software reset
1 Hex			Software reset only
2 Hex		Ring Mode	Phase Z + software reset
3 Hex			Software reset only
4 Hex	500 KHz	Linear Mode	Phase Z + software reset
5 Hex			Software reset only
6 Hex		Ring Mode	Phase Z + software reset
7 Hex			Software reset only

Usage

High-speed counters are programmed as follows:

- The count operation is started as soon as valid settings are made.

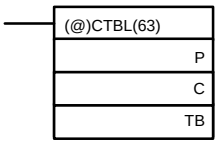
- The PV is reset to 0 when power is turned ON and when program execution is started or stopped.
- The count operation alone does not start the comparison operation with the comparison table.
- The PV can be monitored using the words shown in the following table.

High-speed counter	Word	
	Slot 1	Slot 2
High-speed counter 1	IR 200, IR 201	IR 232, IR 233
High-speed counter 2	IR 202, IR 203	IR 234, IR 235
High-speed counter 3	IR 204, IR 205	IR 236, IR 237
High-speed counter 4	IR 206, IR 207	IR 238, IR 239

Starting Comparison Operation

The comparison table is registered in the CQM1H and the comparison started with CTBL(63). Comparison can also be started using the relevant control bits (IR 21208 to IR 21211 for slot 1 AR 0508 to AR 0511 for slot 2).

Starting Comparison with CTBL(63)



P: Port

C: Mode
000: Target value table registration and comparison start
001: Range comparison table registration and comparison start
002: Target value table registration only
003: Range comparison table registration only

TB: First word of comparison table

High-speed counter	Value specified in P	
	Slot 1	Slot 2
High-speed counter 1	101	001
High-speed counter 2	102	002
High-speed counter 3	103	003
High-speed counter 4	104	004

Setting 000 as the value of C registers a target value comparison table, and setting 001 registers a range comparison table. Comparison begins upon completion of this registration. While comparison is being executed, a bit pattern is stored as internal output bits and external output bits, as determined by the comparison table. Refer to the description of CTBL(63) for details on comparison table registration.

Note Although setting the value of C to 002 registers a target value comparison table, and setting C to 003 registers a range comparison table, comparison does not start automatically for these values. A control bit or INI(61) must be used to start the comparison operation.

Starting Comparison with Control Bits

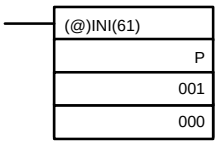
The comparison operation will start when the bit corresponding to the high-speed counter in IR 21208 to IR 21211 for slot 1 or AR 0508 to AR 0511 for slot 2 is turned ON. It is necessary to have registered a comparison table beforehand. Comparisons cannot be performed in PROGRAM mode.

Note The High-speed Counter Board outputs the results of comparison as bit patterns to specific bits in memory, and does not execute interrupt subroutines. Bit patterns consist of internal bits and external bits, and the external bits are output on external output 1 to 4.

Stopping Comparison Operation

To halt a comparison operation, execute INI(61) as shown below. Halting a comparison can also be accomplished using a control bit.

Stopping Comparison with INI(61)



High-speed counter	Value set in P	
	Slot 1	Slot 2
High-speed counter 1	101	001
High-speed counter 2	102	002
High-speed counter 3	103	003
High-speed counter 4	104	004

Stopping Comparison with Control Bits

The comparison operation will stop when the bit corresponding to the high-speed counter in IR 21208 to IR 21211 for slot 1 or AR 0508 to AR 0511 for slot 2 is turned OFF.

Note
1. To restart a comparison, either execute INI(61) with the port number as the first operand and 000 (execute comparison) as the second operand, or change the status of the control bit from 0 to 1.
2. Once a table has been registered, it is retained in the CQM1H throughout the operation (i.e., while a program is running) until a new table is registered.

Reading the PVs

The following two methods can be used to read the PVs of the high-speed counters 1 to 4:

- Reading the PV words in memory
- Using PRV(62)

Reading PV Words in Memory

The PVs of high-speed counters 1 to 4 are stored in memory in the following way. The form in which the PV data is stored is determined by the setting of bits 00 to 03 of DM 6602 for slot 1, and DM 6611 for slot 2. The default setting is 8-digit hexadecimal.

Slot 1:

	Leftmost four digits	Rightmost four digits
Port 1	IR 201	IR 200
Port 2	IR 203	IR 202
Port 3	IR 205	IR 204
Port 4	IR 207	IR 206

	Linear Mode	Ring Mode
8-digit Hex	F8000000 to 07FFFFFF Hex	00000000 to 07FFFFFF Hex
8-digit BCD	F8388608 to 08388607	00000000 to 08388607

(The leftmost digit will be F if the number is negative.)

Slot 2:

	Leftmost four digits	Rightmost four digits
Port 1	IR 233	IR 232
Port 2	IR 235	IR 234
Port 3	IR 237	IR 236
Port 4	IR 239	IR 238

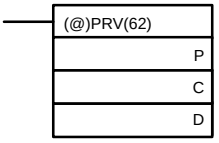
	Linear Mode	Ring Mode
8-digit Hex	F8000000 to 07FFFFFF Hex	00000000 to 07FFFFFF Hex
8-digit BCD	F8388608 to 08388607	00000000 to 08388607

(The leftmost digit will be F if the number is negative.)

Note These words are refreshed only once every cycle, so the value read may differ slightly from the actual PV.

Using PRV(62)

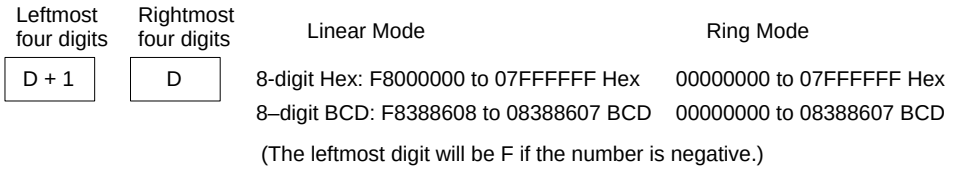
PRV(62) can also be used to read the PVs of high-speed counters 1 to 4.



P: Port
C: 000
D: First destination word

High-speed counter No.	Value specified in P	
	Slot 1	Slot 2
High-speed counter 1	101	001
High-speed counter 2	102	002
High-speed counter 3	103	003
High-speed counter 4	104	004

The PVs of high-speed counters 1 to 4 are stored as shown in the following diagram.



Note PRV(62) reads the current PV when it is executed.

Changing PVs

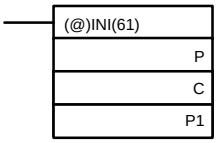
The following 2 methods can be used to change the PVs of high-speed counters 1 to 4:

- Reset the counter (i.e., setting the counter to 0) using one of the reset methods
- Using INI(61)

The following is an explanation of the use of INI(61). Refer to *Reset Methods* on page 65 for an explanation of the use of the reset methods.

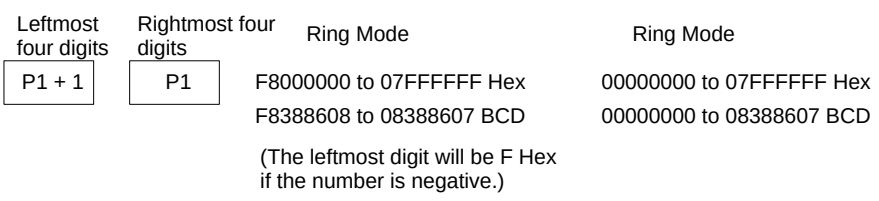
Changing PV with INI(61)

INI(61) is used to change the PV of high-speed counters 1 to 4.



P: Port specifier
C: 002
P1: First PV word

High-speed counter No.	Value specified in P	
	Slot 1	Slot 2
High-speed counter 1	101	001
High-speed counter 2	102	002
High-speed counter 3	103	003
High-speed counter 4	104	004



Note After matching the final target value in a target value comparison table, the comparison process returns automatically to the first target value in the table. There-

fore, following completion of a sequence of comparisons, the process can be repeated by initializing the PV.

Stopping and Restarting the Counting Operation

It is possible to stop the counting operation of one of the high-speed counters 1 to 4 by turning ON a control bit. The PV of the counter will be retained.

The counting operation can be stopped by turning ON bits 12 to 15 of IR 212 for slot 1 or AR 05 for slot 2. These bits correspond to high-speed counters 1 to 4. Turn OFF these bits to restart the counting operation. The high-speed counter will restart from the value at which it was stopped.

Note The Counter Operating Flag can be used to determine whether the count operation is running or stopped (0: Stopped; 1: Operating).

High-speed counter	Counter Operating Flag	
	Slot 1	Slot 2
High-speed counter 1	IR 20812	IR 24012
High-speed counter 2	IR 20912	IR 24112
High-speed counter 3	IR 21012	IR 24212
High-speed counter 4	IR 21112	IR 24312

Examples

The following example illustrates the use of high-speed counter 1 on a High-speed Counter Board mounted in slot 2. Target value comparison is performed to turn ON bits in the internal/external bit patterns stored in memory according to the PV of the counter. The status of the internal output bits is used to control the frequency of a contact pulse output.

The Reset Bit is kept ON in the program so that the PV of the counter is reset on the phase Z signal after the last target value has been reached.

Before running the program, the PC Setup should be set as shown below, and the CQM1H restarted to enable the new setting in DM 6611.

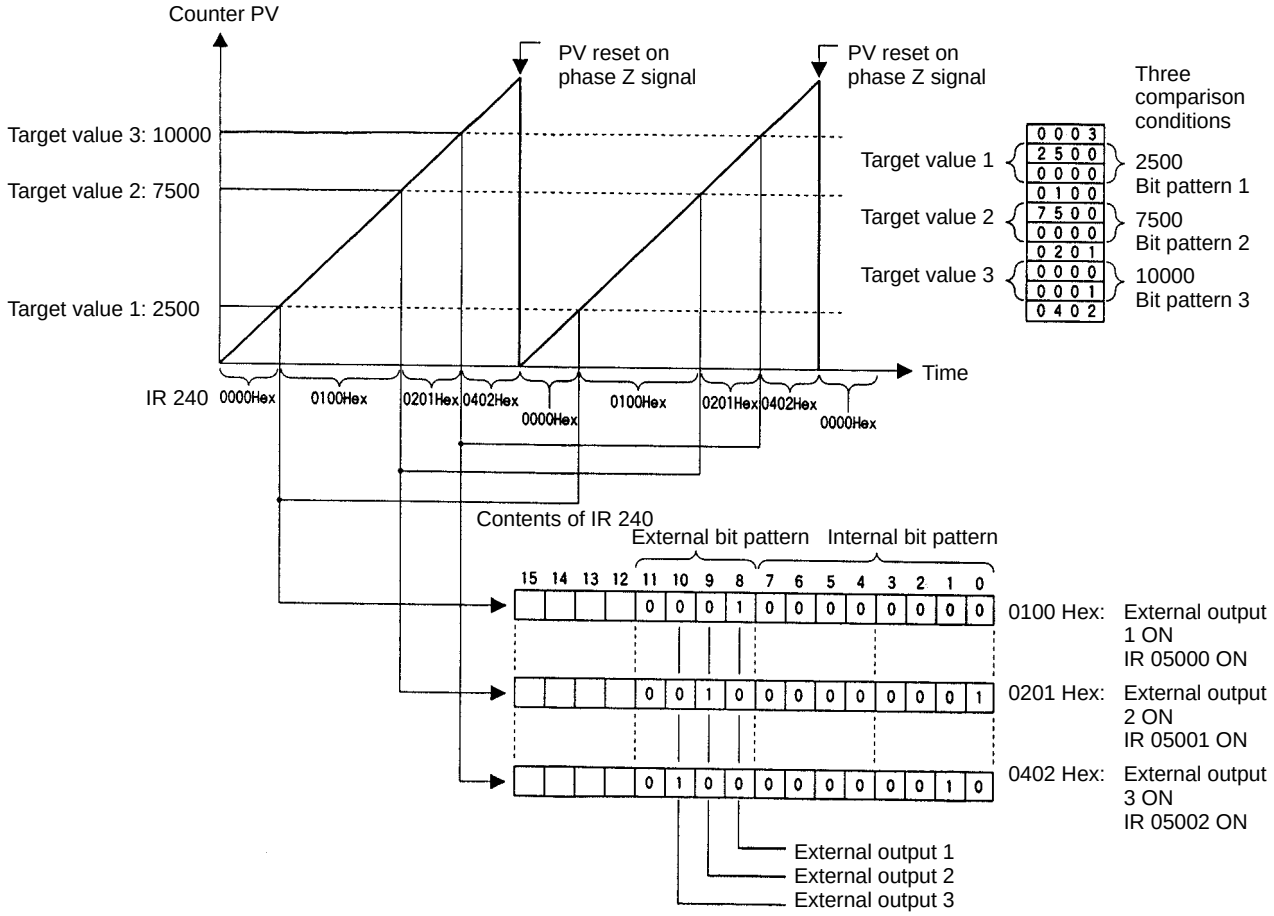
DM 6611: 0001 (Sourcing outputs for external outputs 1 to 4, 8-digit BCD for PV storage of high-speed counters 1 to 4)

DM 6643: 0003 (High-speed counter 1: Count frequency of 50 kHz; Linear Mode; phase-Z signal + software reset; Up/Down Mode).

When the PV reaches 2500, IR 05000 will be turned ON and external output 1 will be turned ON.

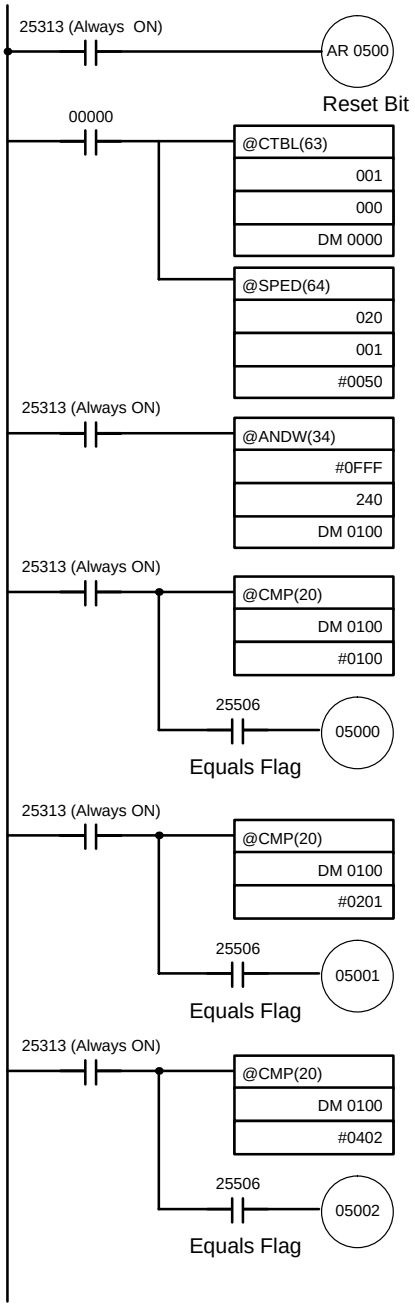
When the PV reaches 7500, IR 05001 will be turned ON and external output 2 will be turned ON.

When the PV reaches 10000, IR 05002 will be turned ON and external output 3 will be turned ON.



As shown in the following programming example, the frequency of the contact pulse output is changed from the value of 500 Hz set when CTBL(63) is execut-

ed to 200 Hz, 100 Hz, and then 0 Hz when IR 05000, IR 05001, and then IR 05002 turn ON.



Keeps the Reset Bit for the high-speed counter ON.

Specifies target comparison for high-speed counter 1 in slot 2,, registers a target value comparison table, and begins comparison starting at DM 0000.

Sets continuous contact pulse output from output position 02 at 500 Hz and starts pulse output.

ANDs the contents of the bit pattern stored in IR 240 and stores the result in DM 0100.

Compares DM 0100 to #0100.

Turns ON IR 05000 if DM 0100 contains #0100.

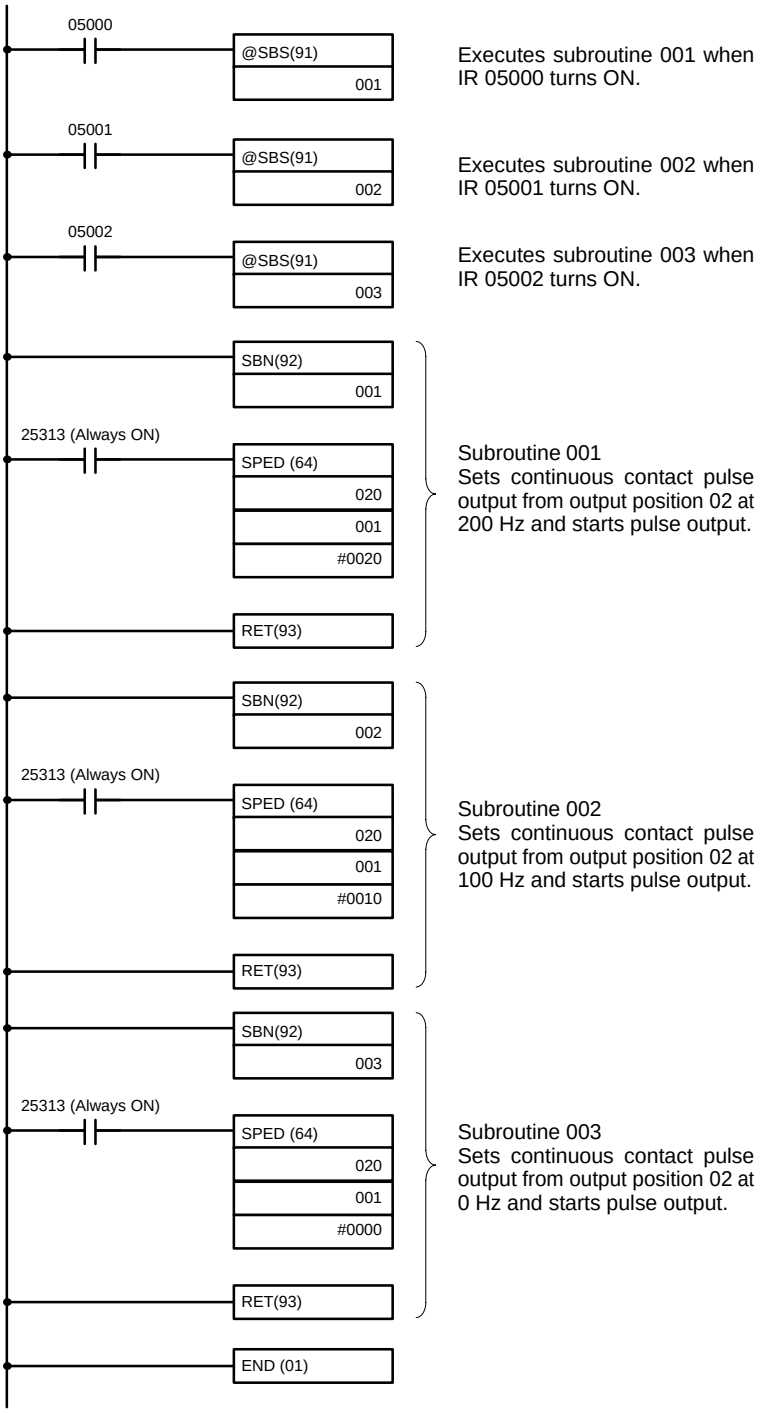
Compares DM 0100 to #0201.

Turns ON IR 05001 if DM 0100 contains #0201.

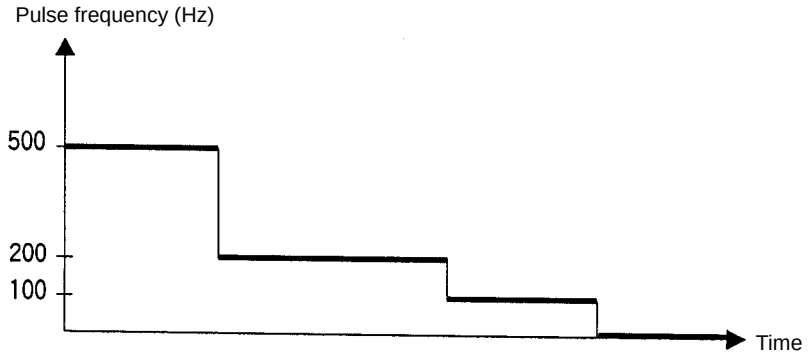
Compares DM 0100 to #0402.

Turns ON IR 05002 if DM 0100 contains #0402.

DM 0000: 0003 — Three comparison conditions
DM 0001: 2500 — Target value: 2,500
DM 0002: 0000
DM 0003: 0100 — Bit pattern (1)
DM 0004: 7500 — Target value: 7,500
DM 0005: 0000
DM 0006: 0201 — Bit pattern (2)
DM 0007: 0000 — Target value 2: 10,000
DM 0008: 0001
DM 0009: 0402 — Bit pattern (3)


05000
@SBS(91)
001
Executes subroutine 001 when IR 05000 turns ON.
05001
@SBS(91)
002
Executes subroutine 002 when IR 05001 turns ON.
05002
@SBS(91)
003
Executes subroutine 003 when IR 05002 turns ON.
SBN(92)
001
25313 (Always ON)
SPED (64)
020
001
#0020
RET(93)
Subroutine 001
Sets continuous contact pulse output from output position 02 at 200 Hz and starts pulse output.
SBN(92)
002
25313 (Always ON)
SPED (64)
020
001
#0010
RET(93)
Subroutine 002
Sets continuous contact pulse output from output position 02 at 100 Hz and starts pulse output.
SBN(92)
003
25313 (Always ON)
SPED (64)
020
001
#0000
RET(93)
Subroutine 003
Sets continuous contact pulse output from output position 02 at 0 Hz and starts pulse output.
END (01)

Operation will be as illustrated below when the program is executed.



2-2 Pulse I/O Board

2-2-1 Model

Name	Model	Specifications
Pulse I/O Board	CQM1H-PLB21	Two pulse input points and two pulse output points

2-2-2 Function

The Pulse I/O Board is an Inner Board that supports two pulse inputs and two pulse outputs.

Pulse Inputs 1 and 2

Pulse inputs 1 and 2 can be used as high-speed counters to count pulses input at either 50 kHz (signal phase) or 25 kHz (differential phase). Interrupt processing can be performed based on the present values (PV) of the counters.

Input Mode

The following three Input Modes are available:

- Differential Phase Mode (4x)
- Pulse/Direction Mode
- Up/Down Mode

Interrupts

The Board can be set to execute an interrupt subroutine when the value of the high-speed counter matches a specified target value, or an interrupt subroutine when the PV falls within a specified comparison range.

Pulse Outputs 1 and 2

Two 10 Hz to 50 kHz pulses can be output from port 1 and port 2. Both fixed and variable duty factors can be used.

- The fixed duty factor can raise or lower the frequency of the output from 10 Hz to 50 kHz smoothly.
- The variable duty factor enables pulse output to be performed using a duty factor ranging from 1% to 99%.

Note While pulse inputs and pulse outputs can be performed simultaneously, it is not possible to use all high-speed counter and pulse output functionality at the same time. The Port Mode Setting (High-speed Counter Mode/Simple Positioning Mode) in the PC Setup (DM 6611) will determines which has full functionality enabled.

Ports 1 and 2

Two pulse inputs (high-speed counter) and two pulse outputs can be used simultaneously via ports 1 and 2. To determine which has functional priority, the appropriate Port Mode setting must be entered in the PC Setup (DM 6611).